OIPE JC180
APR 09 2004
PATENT & TRADEMARK OFFICE

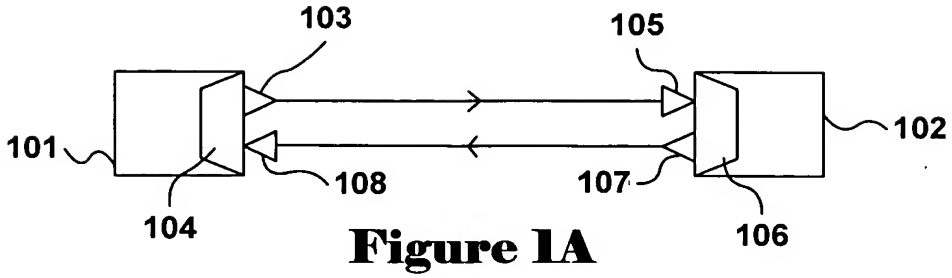


Figure 1A

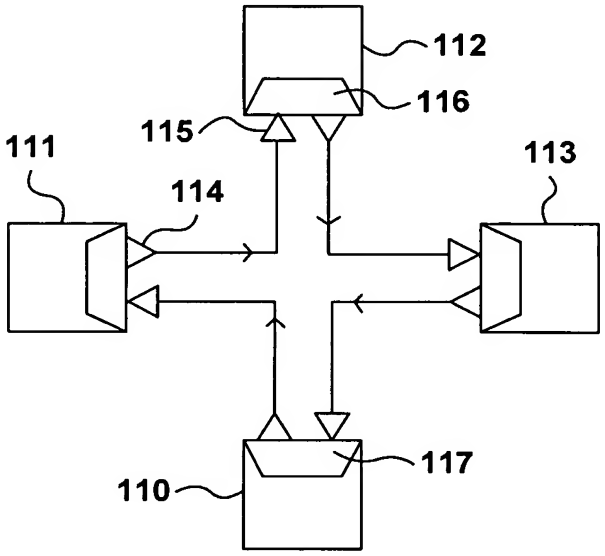


Figure 1B

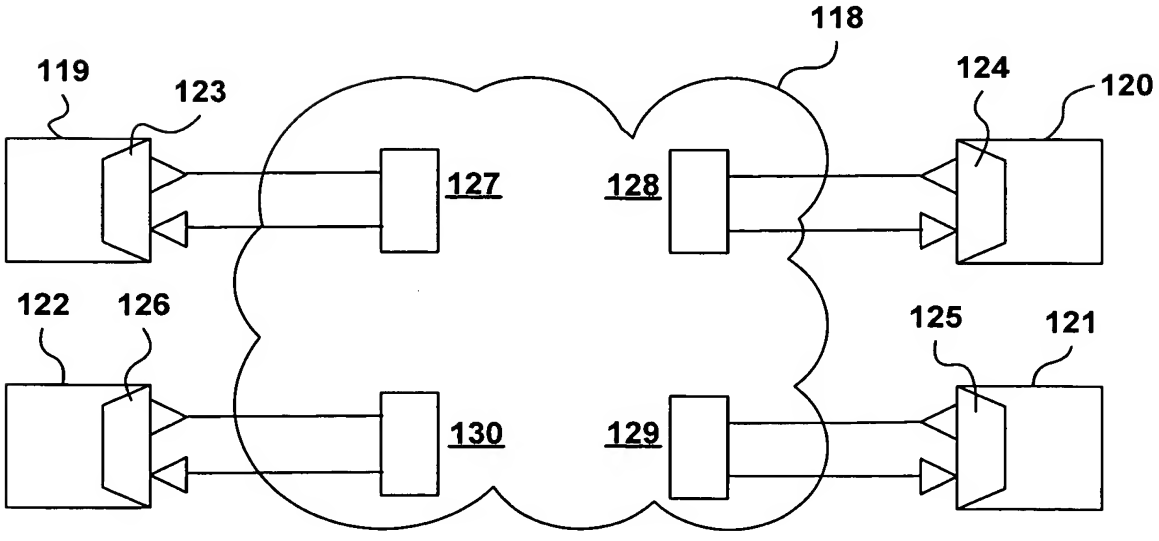


Figure 1C

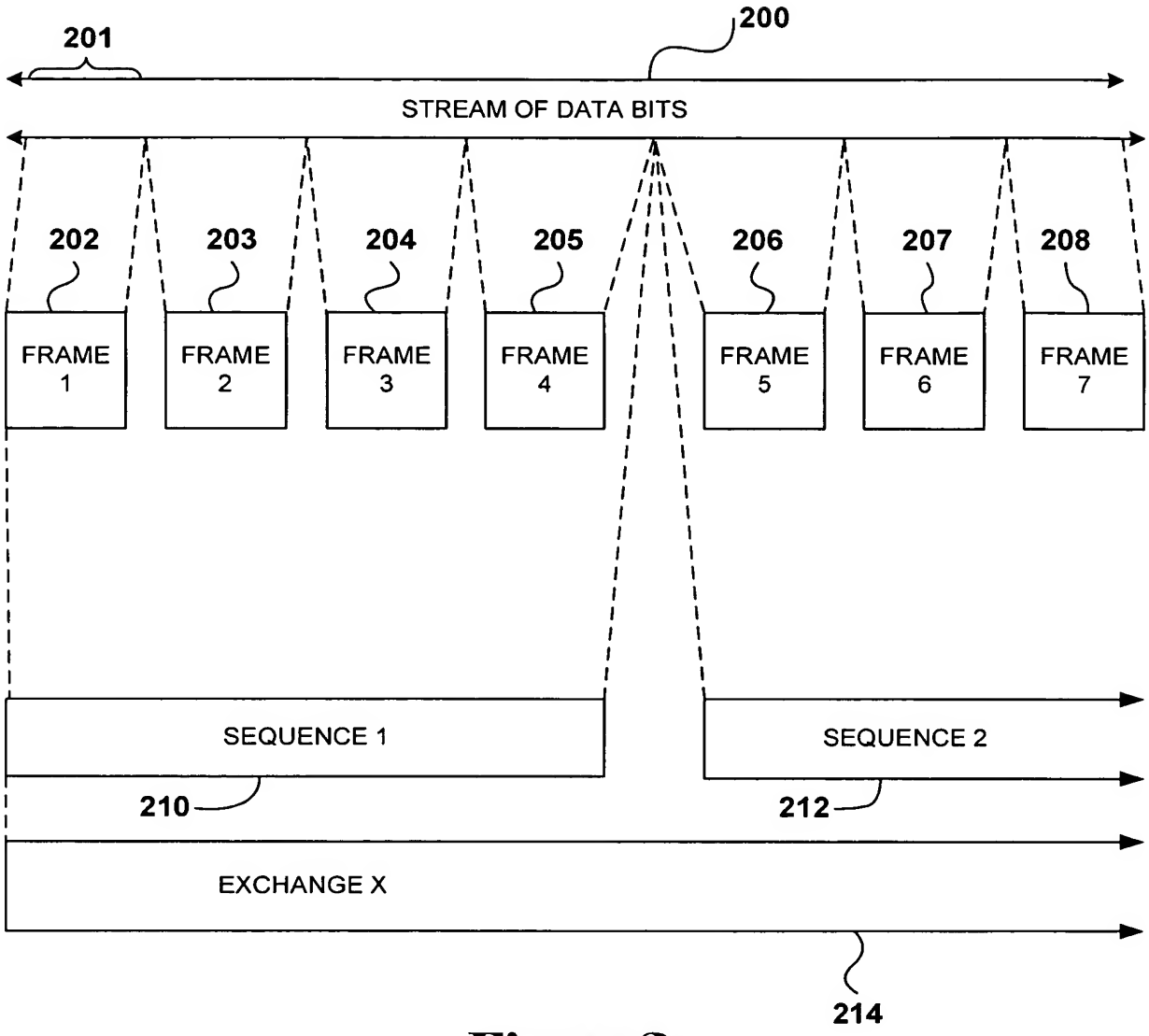

201
200
STREAM OF DATA BITS
202
203
204
205
206
207
208
FRAME 1
FRAME 2
FRAME 3
FRAME 4
FRAME 5
FRAME 6
FRAME 7
SEQUENCE 1
SEQUENCE 2
210
212
EXCHANGE X
214

Figure 2

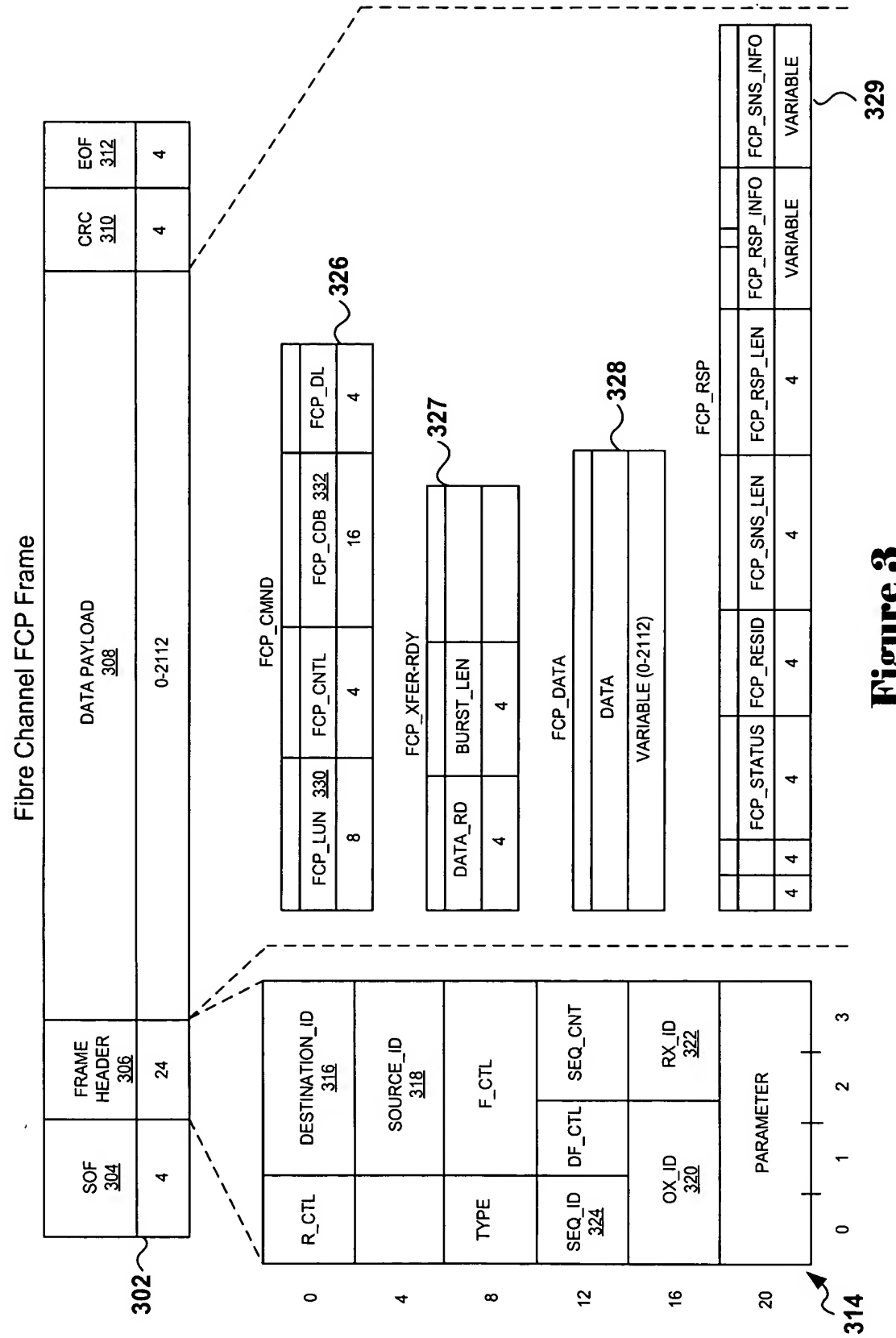

Fibre Channel FCP Frame
SOF 304
FRAME HEADER 306
DATA PAYLOAD 308
CRC 310
EOF 312
4
24
0-2112
4
4
302
R_CTL
DESTINATION_ID 316
SOURCE_ID 318
TYPE
F_CTL
SEQ_ID 324
DF_CTL
SEQ_CNT
OX_ID 320
RX_ID 322
PARAMETER
0
4
8
12
16
20
0
1
2
3
314
FCP_CMND
FCP_LUN 330
FCP_CNTL
FCP_CDB 332
FCP_DL
8
4
16
4
326
FCP_XFER-RDY
DATA_RD
BURST_LEN
4
4
327
FCP_DATA
DATA
VARIABLE (0-2112)
328
FCP_RSP
FCP_STATUS
FCP_RESID
FCP_SNS_LEN
FCP_RSP_LEN
FCP_RSP_INFO
FCP_SNS_INFO
4
4
4
4
4
4
VARIABLE
VARIABLE
329

Figure 3

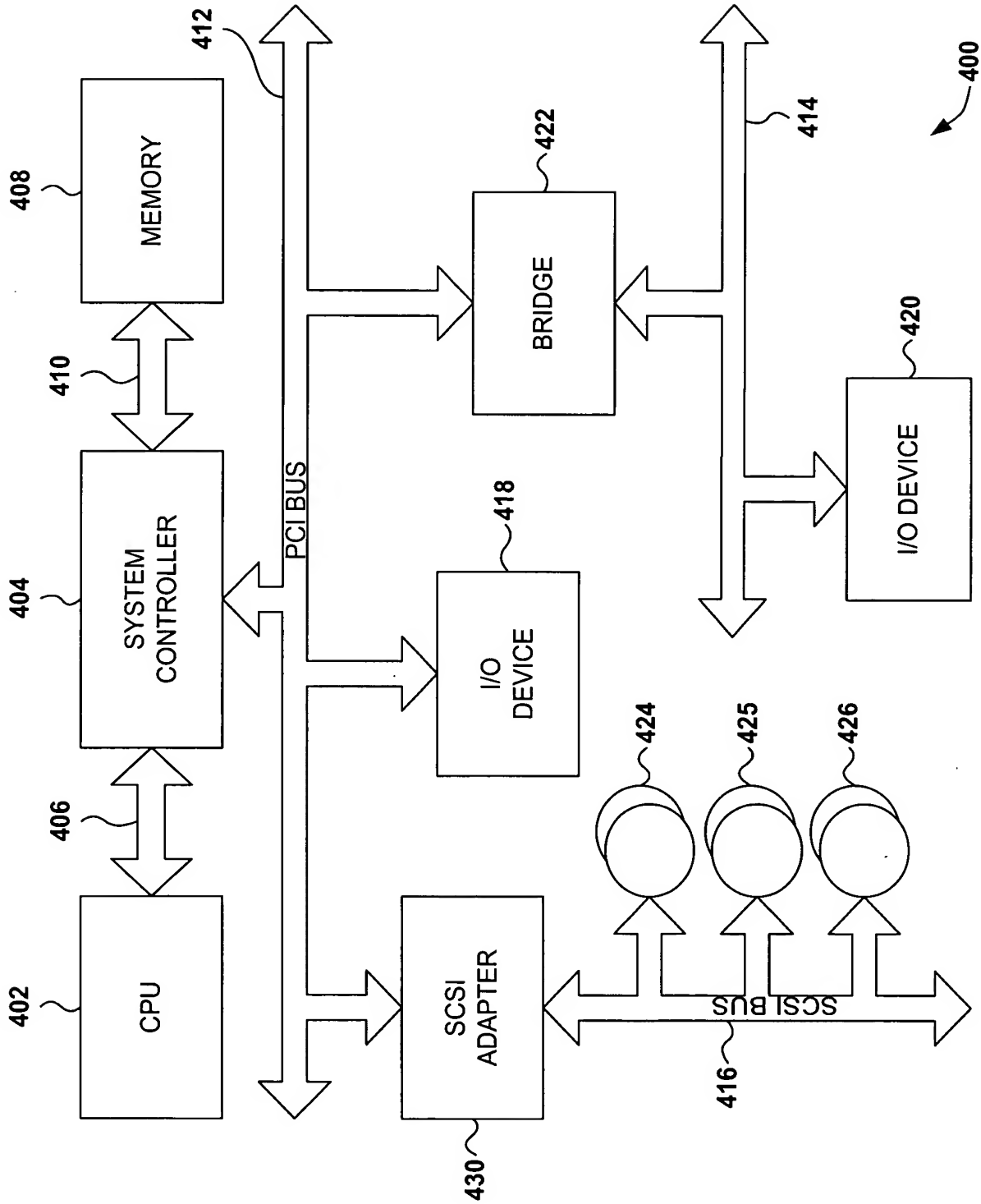

400
402
CPU
406
404
SYSTEM CONTROLLER
410
408
MEMORY
412
PCI BUS
418
I/O DEVICE
422
BRIDGE
414
420
I/O DEVICE
424
425
426
SCSI ADAPTER
SCSI BUS
416
430

Figure 4

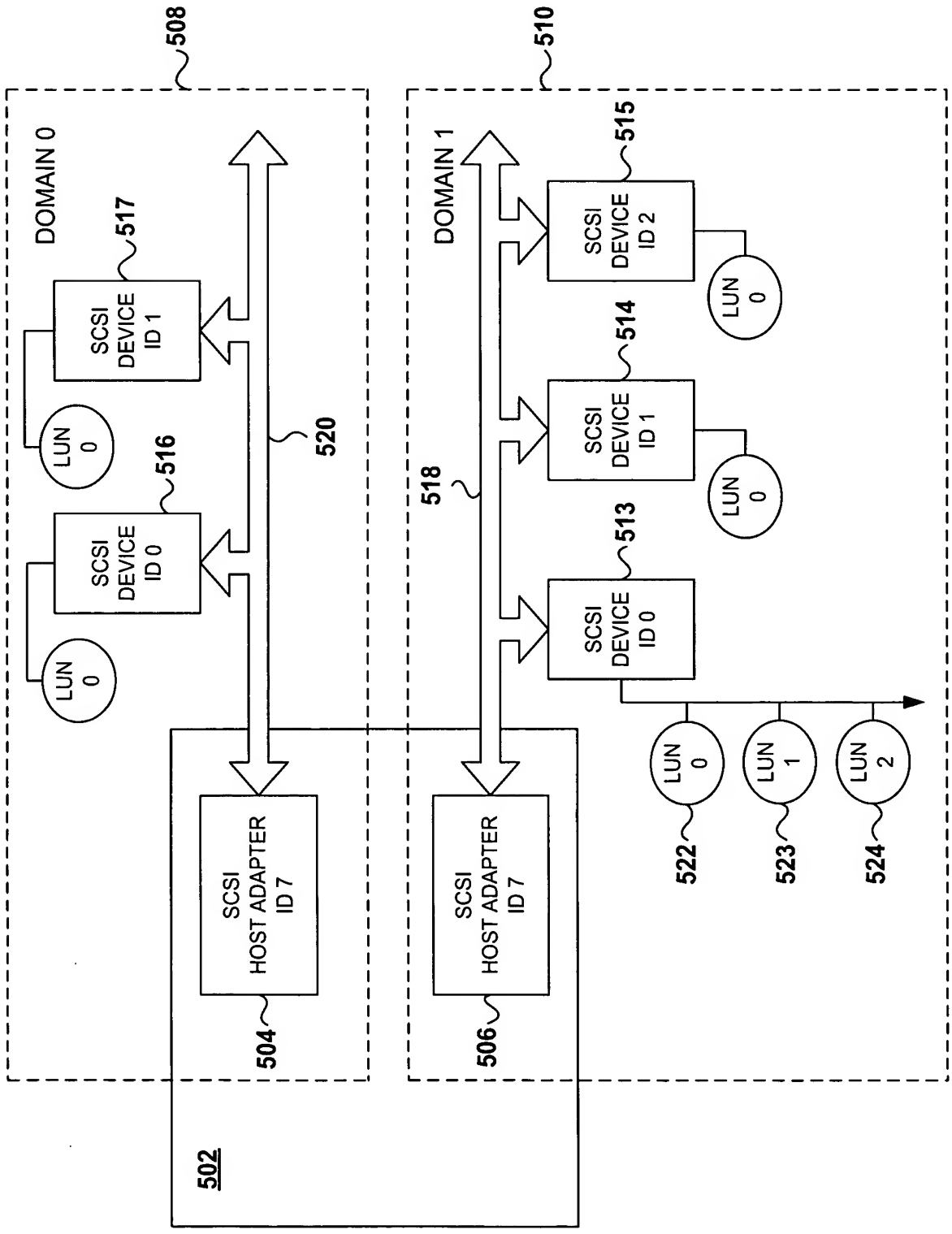

502
DOMAIN 0
508
SCSI HOST ADAPTER ID 7
504
SCSI DEVICE ID 0
516
LUN 0
SCSI DEVICE ID 1
517
LUN 0
520
DOMAIN 1
510
SCSI HOST ADAPTER ID 7
506
518
SCSI DEVICE ID 0
513
LUN 0
LUN 1
LUN 2
522
523
524
SCSI DEVICE ID 1
514
LUN 0
SCSI DEVICE ID 2
515
LUN 0

Figure 5

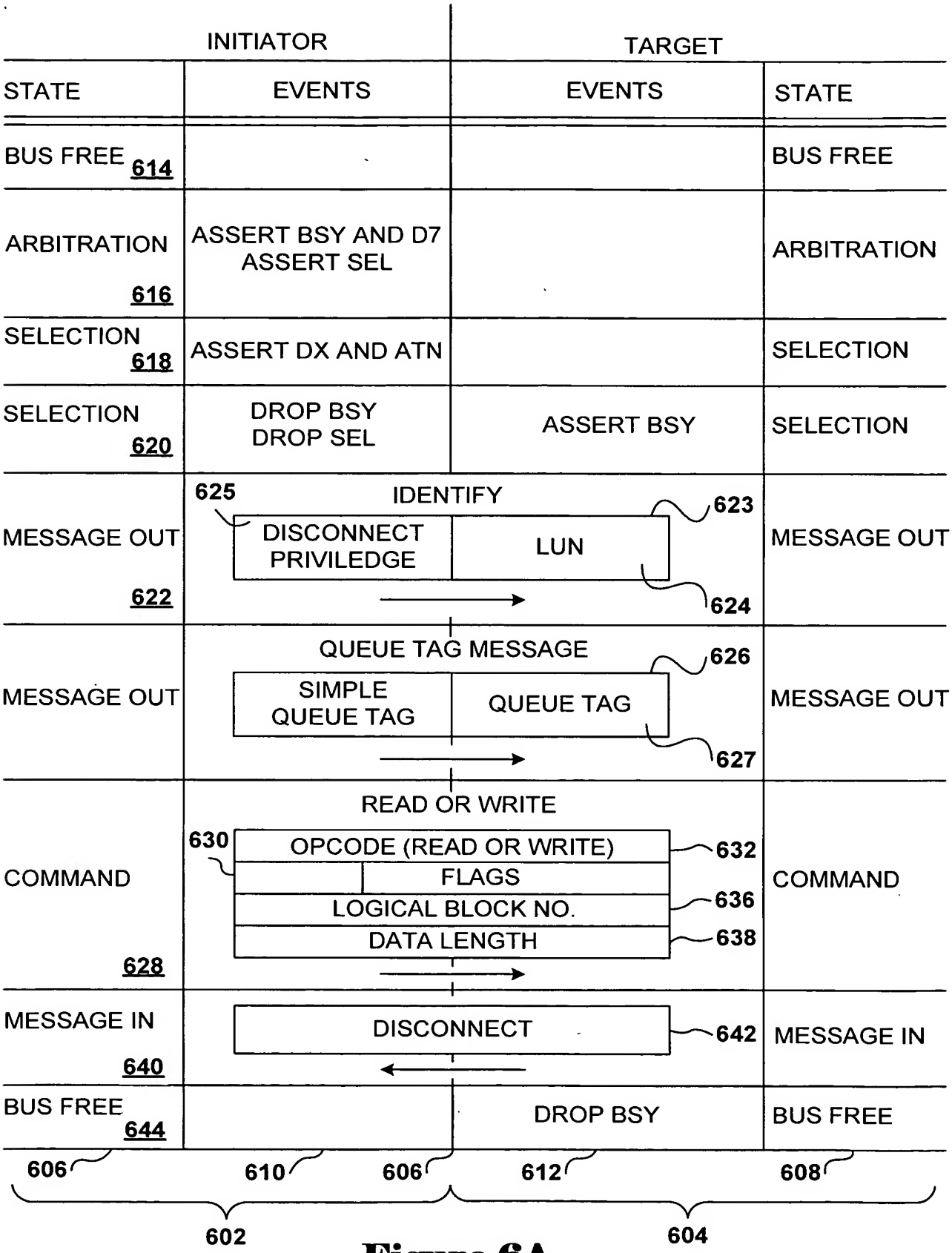

INITIATOR
TARGET
STATE
EVENTS
EVENTS
STATE
BUS FREE 614
BUS FREE
ARBITRATION 616
ASSERT BSY AND D7
ASSERT SEL
ARBITRATION
SELECTION 618
ASSERT DX AND ATN
SELECTION
SELECTION 620
DROP BSY
DROP SEL
ASSERT BSY
SELECTION
MESSAGE OUT 622
625
IDENTIFY
623
DISCONNECT PRIVILEDGE
LUN
624
MESSAGE OUT
MESSAGE OUT
QUEUE TAG MESSAGE
626
SIMPLE QUEUE TAG
QUEUE TAG
627
MESSAGE OUT
COMMAND 628
READ OR WRITE
630
OPCODE (READ OR WRITE)
632
FLAGS
LOGICAL BLOCK NO.
636
DATA LENGTH
638
COMMAND
MESSAGE IN 640
DISCONNECT
642
MESSAGE IN
BUS FREE 644
DROP BSY
BUS FREE
606
610
606
612
608
602
604

Figure 6A

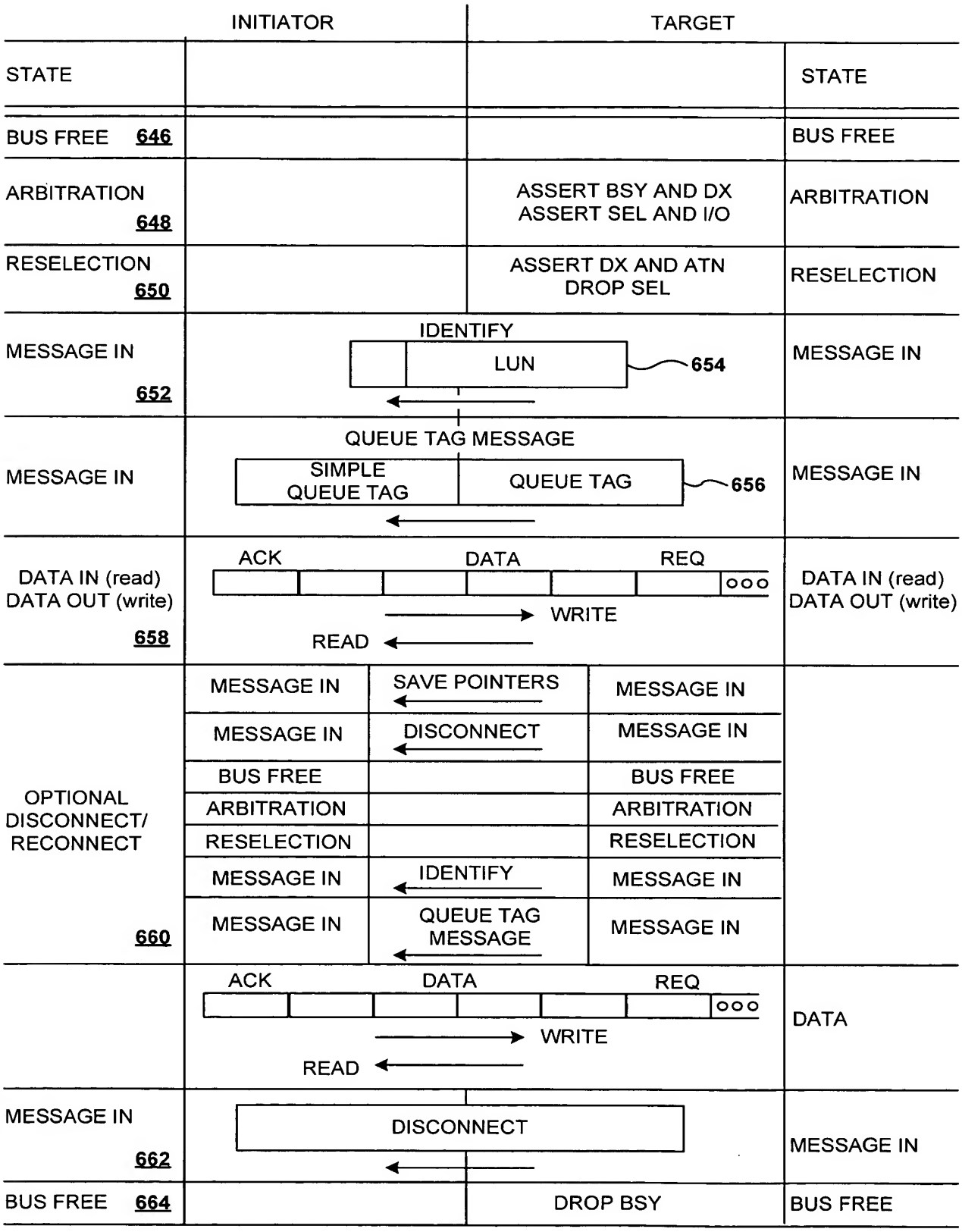

INITIATOR
TARGET
STATE
STATE
BUS FREE 646
BUS FREE
ARBITRATION 648
ASSERT BSY AND DX
ASSERT SEL AND I/O
ARBITRATION
RESELECTION 650
ASSERT DX AND ATN
DROP SEL
RESELECTION
MESSAGE IN 652
IDENTIFY
LUN
654
MESSAGE IN
MESSAGE IN
QUEUE TAG MESSAGE
SIMPLE QUEUE TAG
QUEUE TAG
656
MESSAGE IN
DATA IN (read)
DATA OUT (write) 658
ACK
DATA
REQ
WRITE
READ
DATA IN (read)
DATA OUT (write)
OPTIONAL DISCONNECT/ RECONNECT 660
MESSAGE IN
SAVE POINTERS
MESSAGE IN
MESSAGE IN
DISCONNECT
MESSAGE IN
BUS FREE
BUS FREE
ARBITRATION
ARBITRATION
RESELECTION
RESELECTION
MESSAGE IN
IDENTIFY
MESSAGE IN
MESSAGE IN
QUEUE TAG MESSAGE
MESSAGE IN
ACK
DATA
REQ
WRITE
READ
DATA
MESSAGE IN 662
DISCONNECT
MESSAGE IN
BUS FREE 664
DROP BSY
BUS FREE

Figure 6B

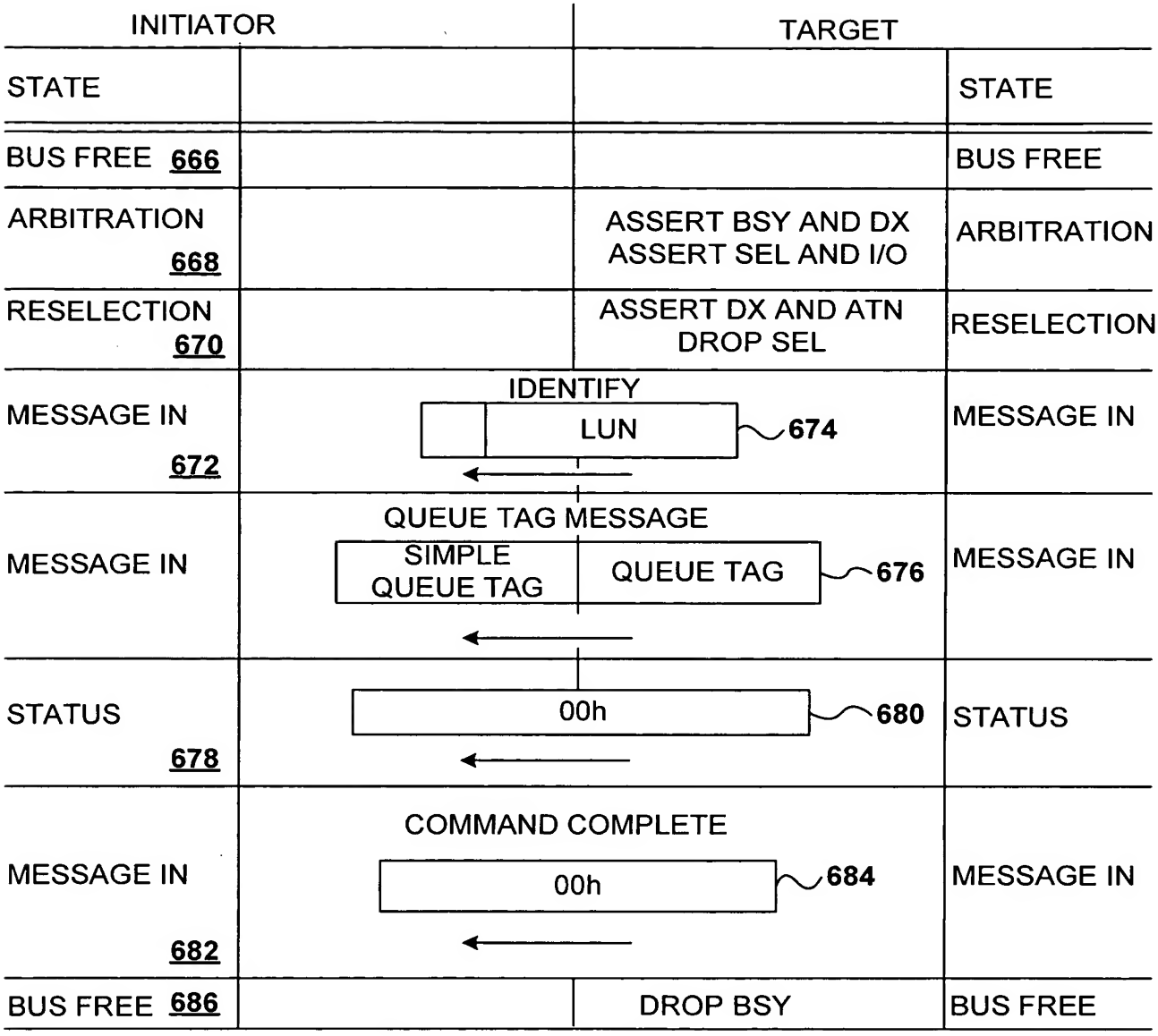

INITIATOR
TARGET
STATE
STATE
BUS FREE 666
BUS FREE
ARBITRATION 668
ASSERT BSY AND DX
ASSERT SEL AND I/O
ARBITRATION
RESELECTION 670
ASSERT DX AND ATN
DROP SEL
RESELECTION
MESSAGE IN 672
IDENTIFY
LUN
674
MESSAGE IN
MESSAGE IN
QUEUE TAG MESSAGE
SIMPLE QUEUE TAG
QUEUE TAG
676
MESSAGE IN
STATUS 678
00h
680
STATUS
MESSAGE IN 682
COMMAND COMPLETE
00h
684
MESSAGE IN
BUS FREE 686
DROP BSY
BUS FREE

Figure 6C

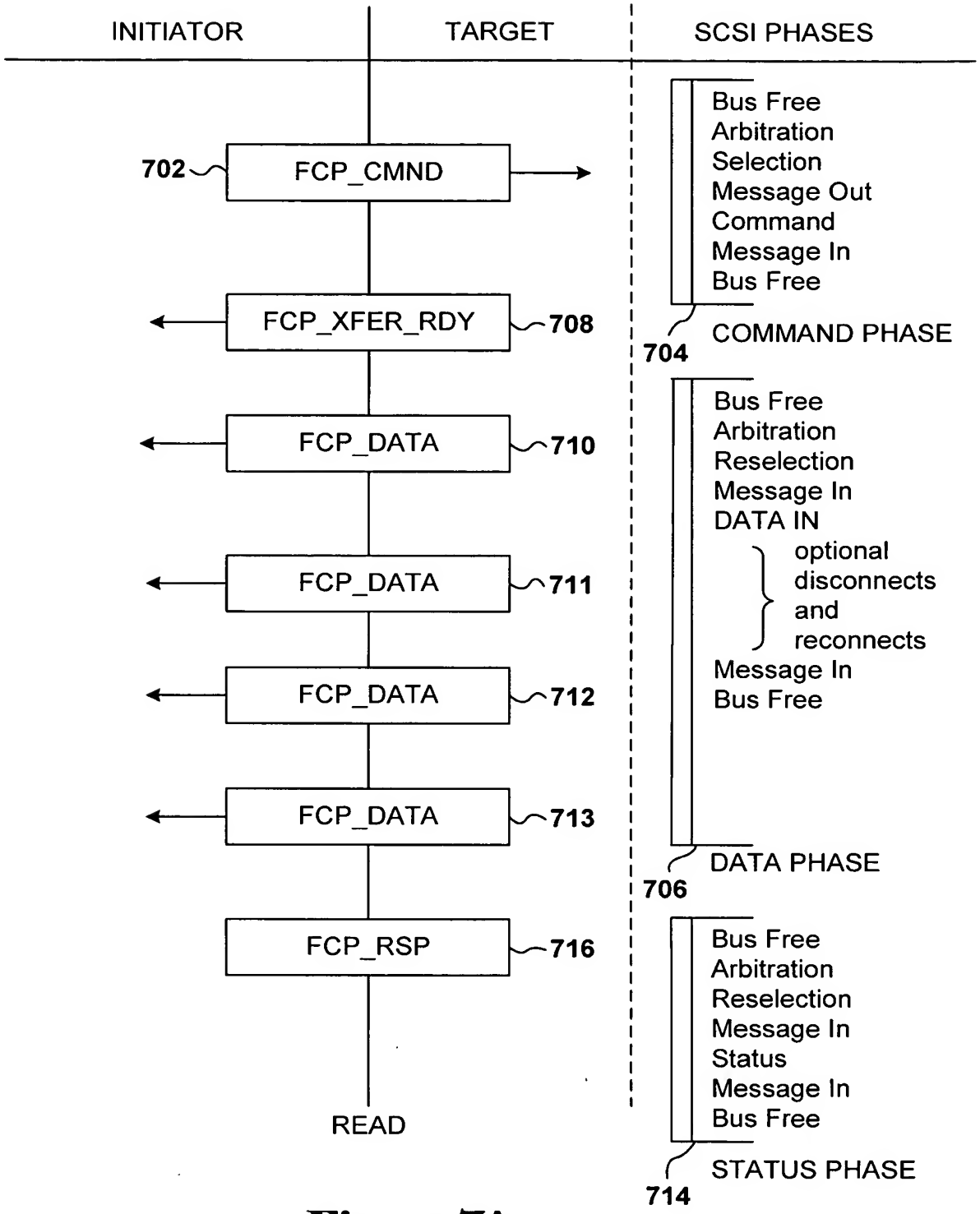

INITIATOR
TARGET
SCSI PHASES
702
FCP_CMND
FCP_XFER_RDY
708
FCP_DATA
710
FCP_DATA
711
FCP_DATA
712
FCP_DATA
713
FCP_RSP
716
READ
Bus Free
Arbitration
Selection
Message Out
Command
Message In
Bus Free
COMMAND PHASE
704
Bus Free
Arbitration
Reselection
Message In
DATA IN
optional
disconnects
and
reconnects
Message In
Bus Free
DATA PHASE
706
Bus Free
Arbitration
Reselection
Message In
Status
Message In
Bus Free
STATUS PHASE
714

Figure 7A

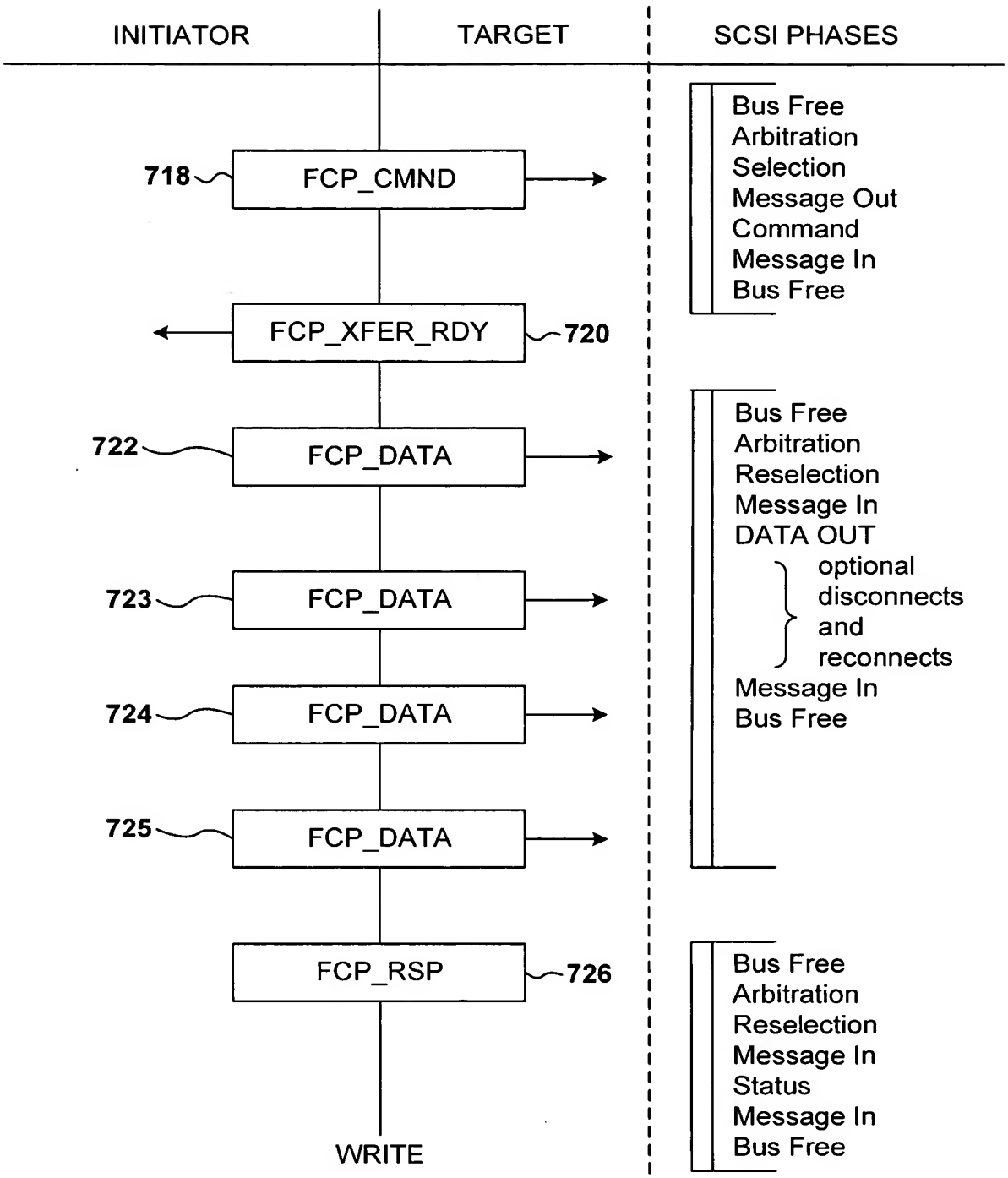

INITIATOR
TARGET
SCSI PHASES
718
FCP_CMND
Bus Free
Arbitration
Selection
Message Out
Command
Message In
Bus Free
FCP_XFER_RDY
720
722
FCP_DATA
Bus Free
Arbitration
Reselection
Message In
DATA OUT
optional disconnects and reconnects
Message In
Bus Free
723
FCP_DATA
724
FCP_DATA
725
FCP_DATA
FCP_RSP
726
Bus Free
Arbitration
Reselection
Message In
Status
Message In
Bus Free
WRITE

Figure 7B

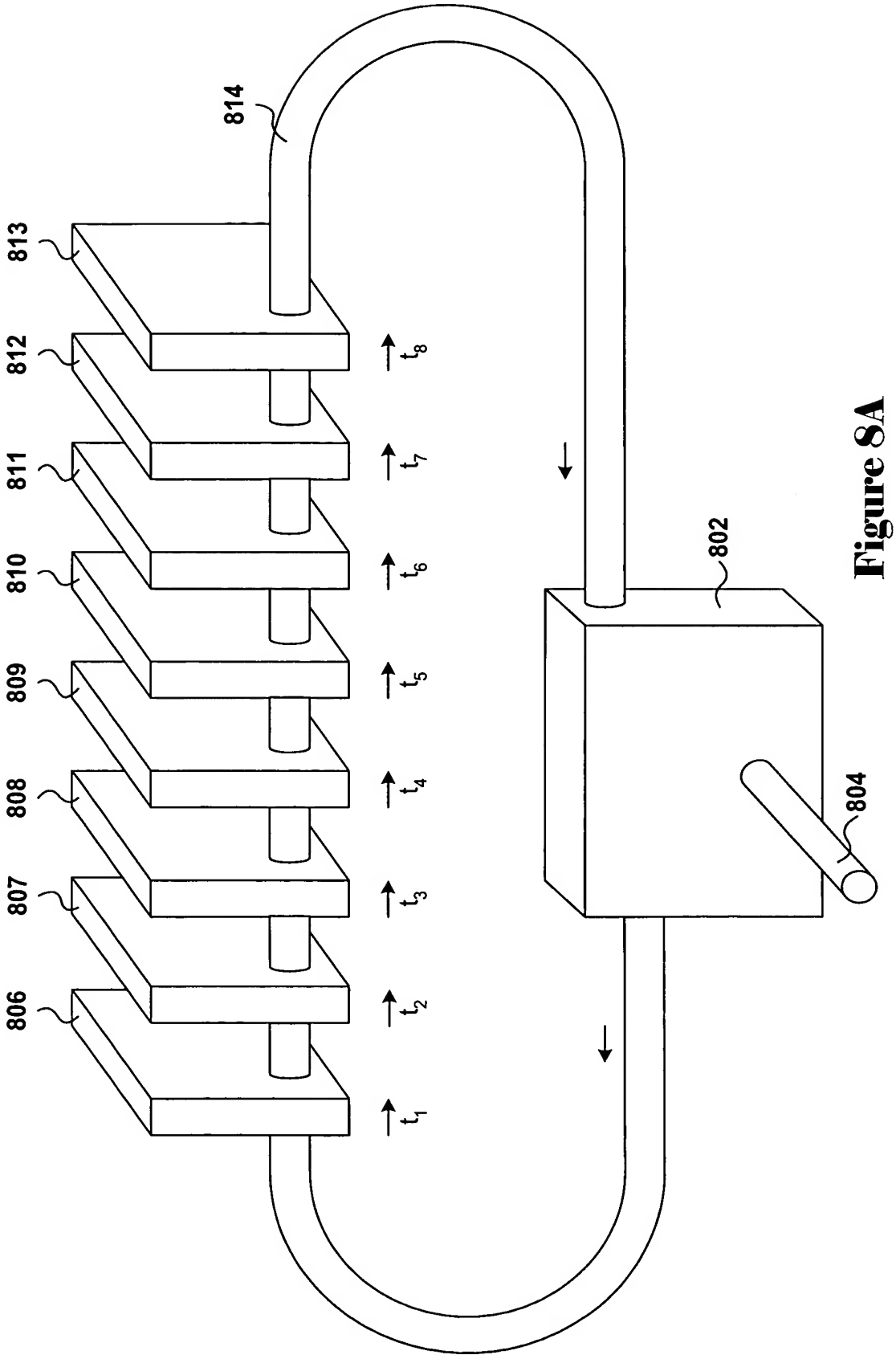


Figure 8A

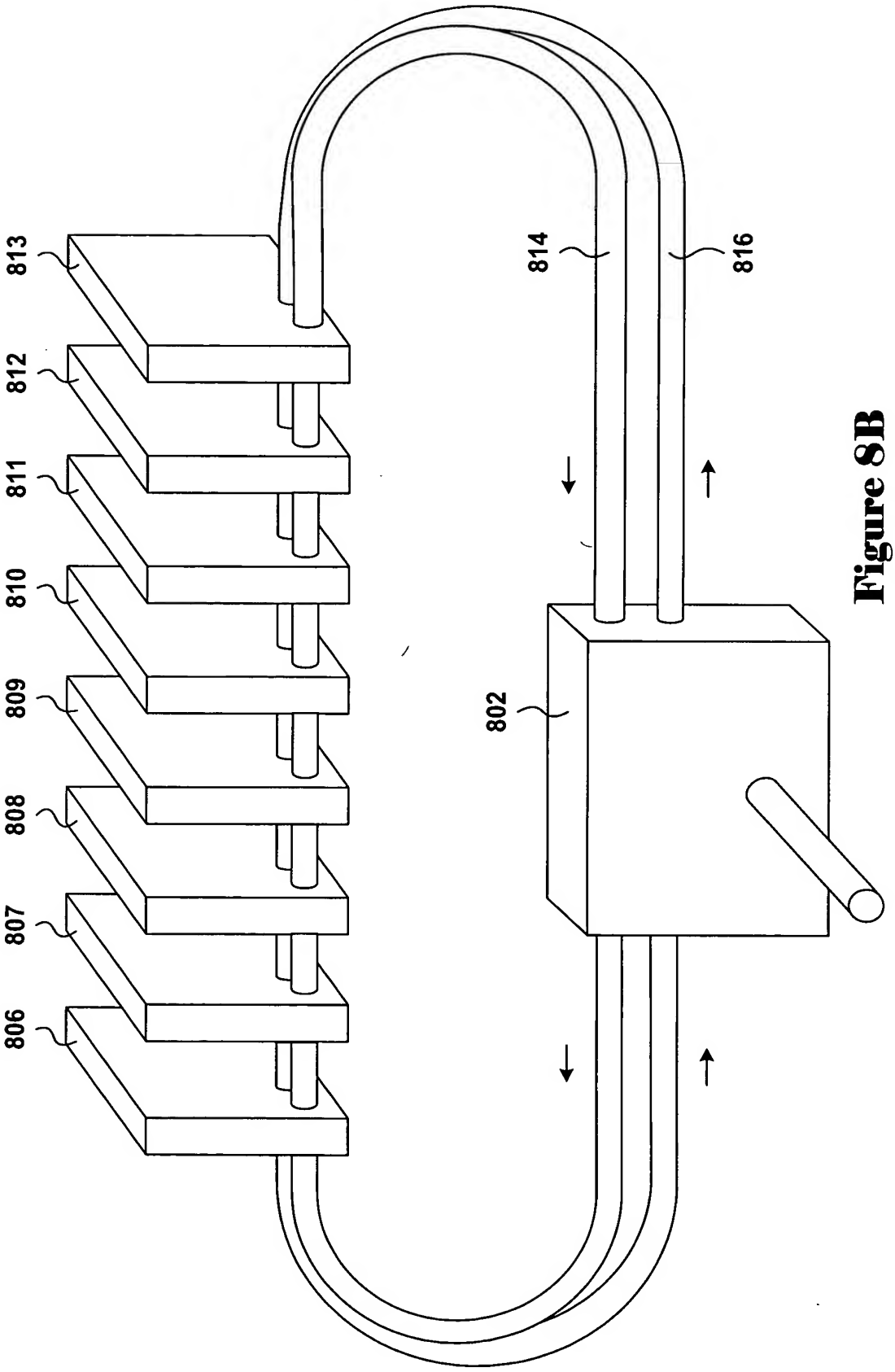


Figure 8B

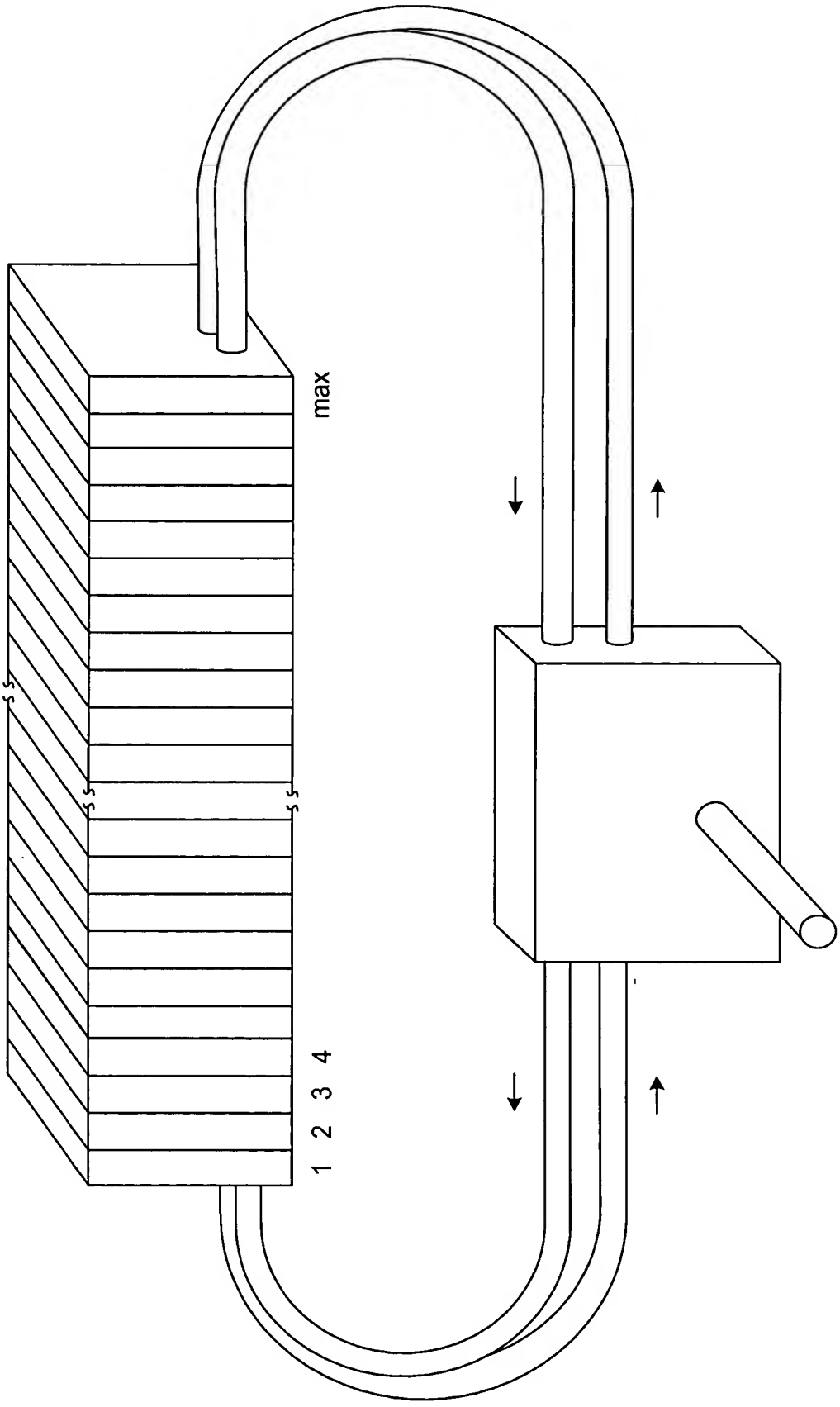


Figure 8C

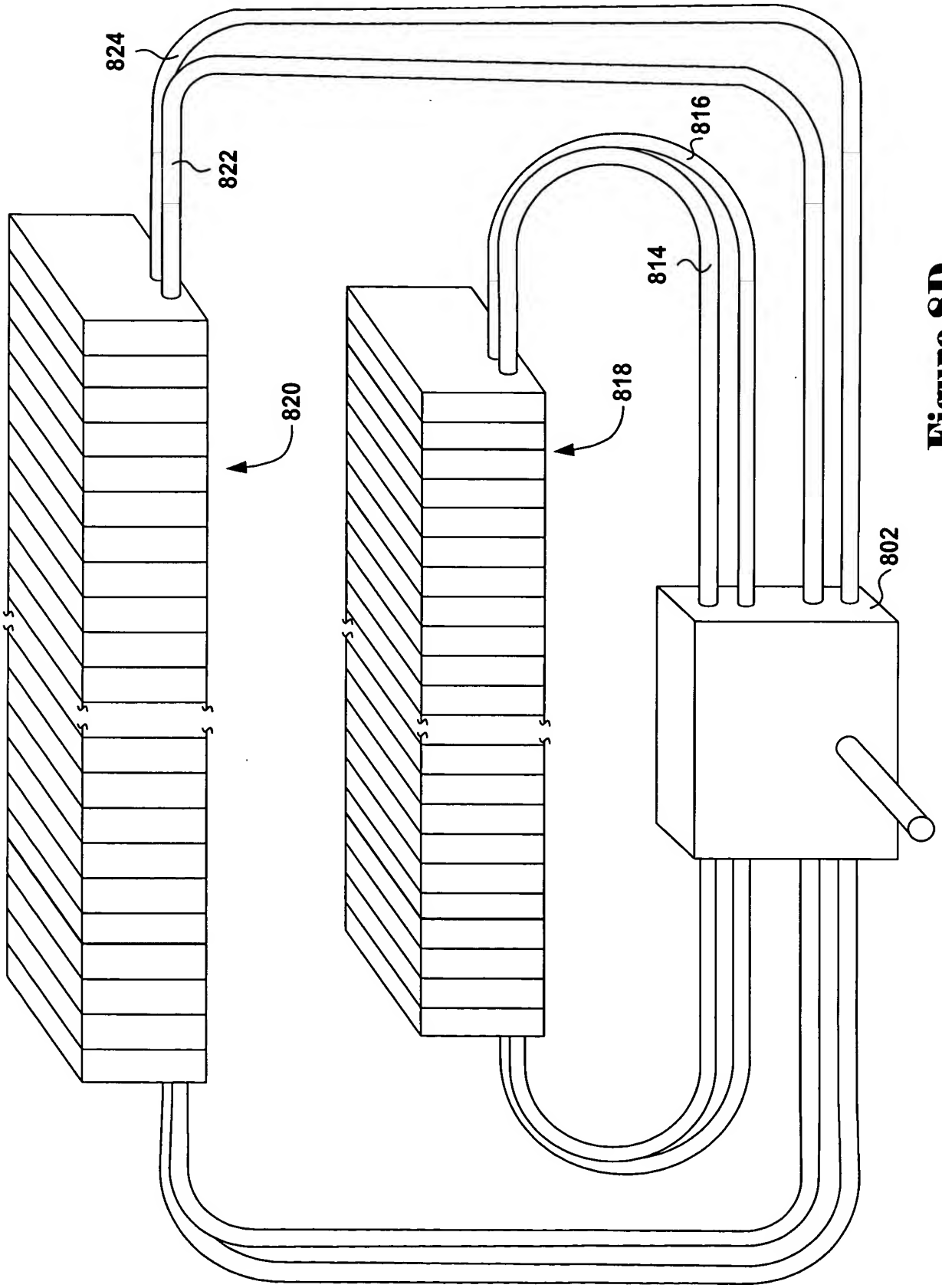


Figure 8D

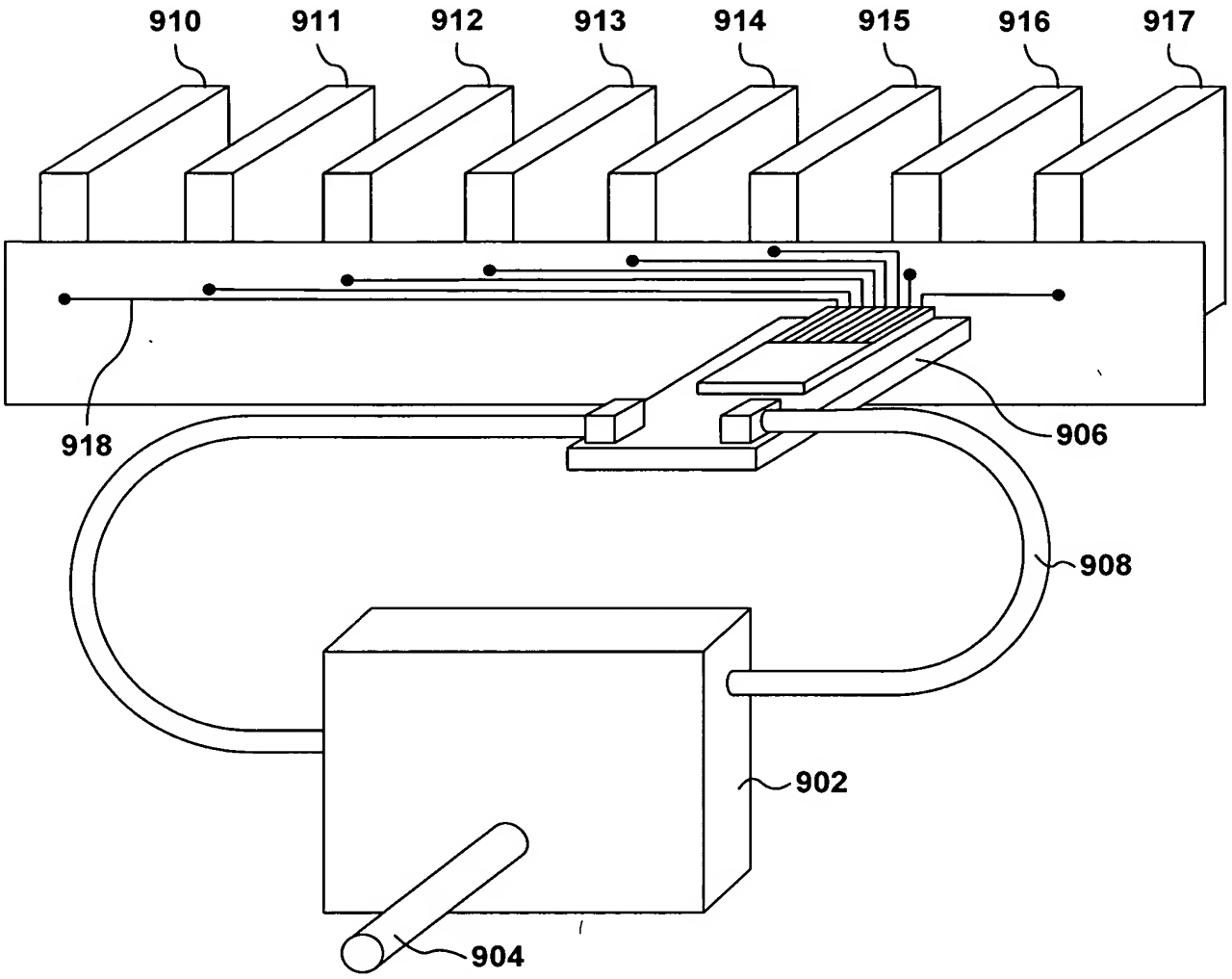


Figure 9

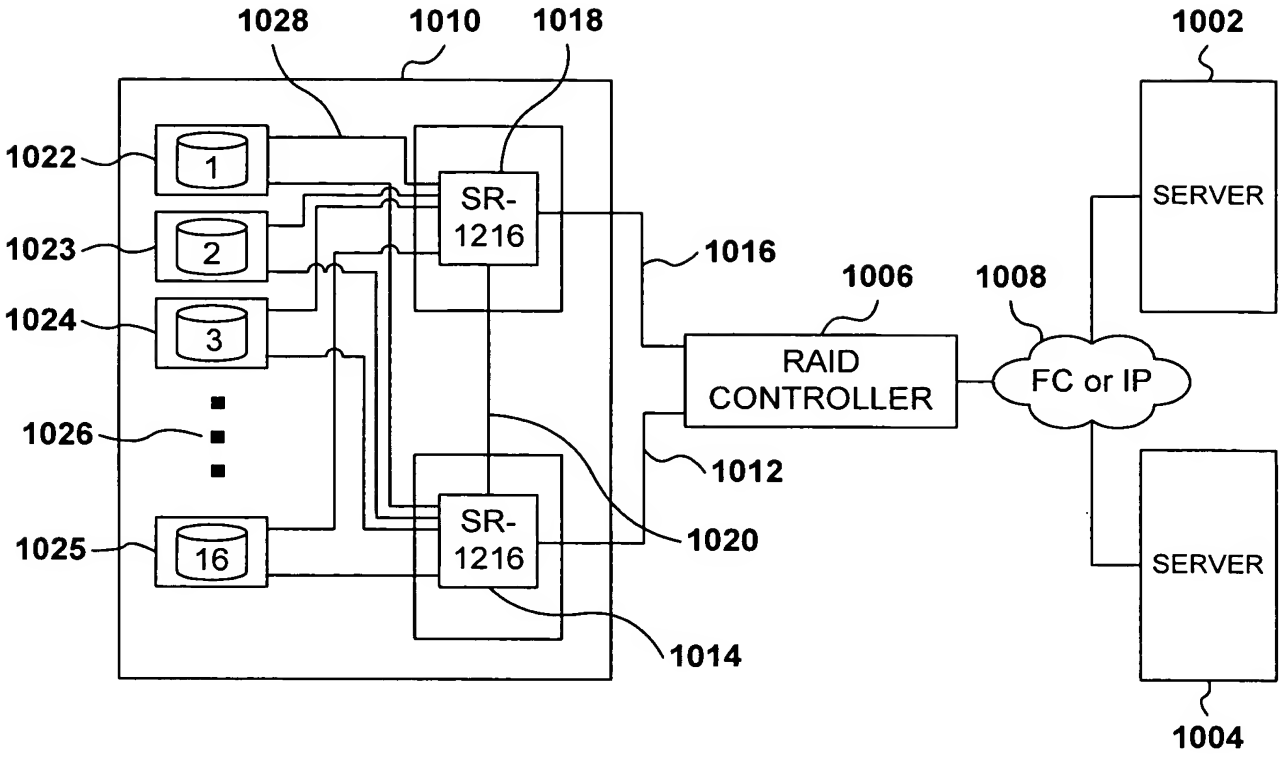

1028
1010
1018
1002
1022
1
SR-
1216
SERVER
1023
2
1016
1006
1008
1024
3
RAID
CONTROLLER
FC or IP
1026
1012
1020
1025
16
SR-
1216
SERVER
1014
1004

FIGURE 10

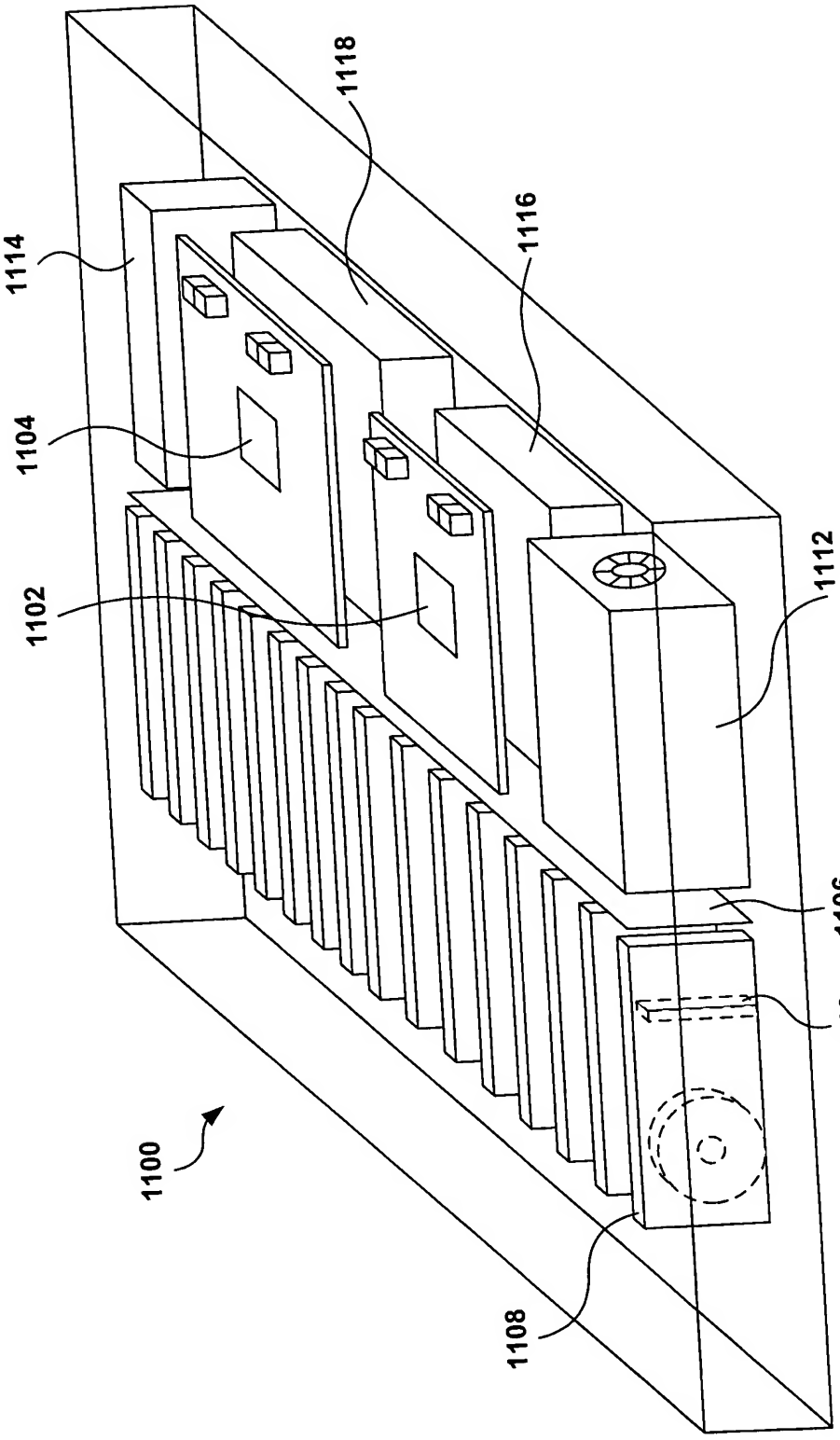


Figure 11

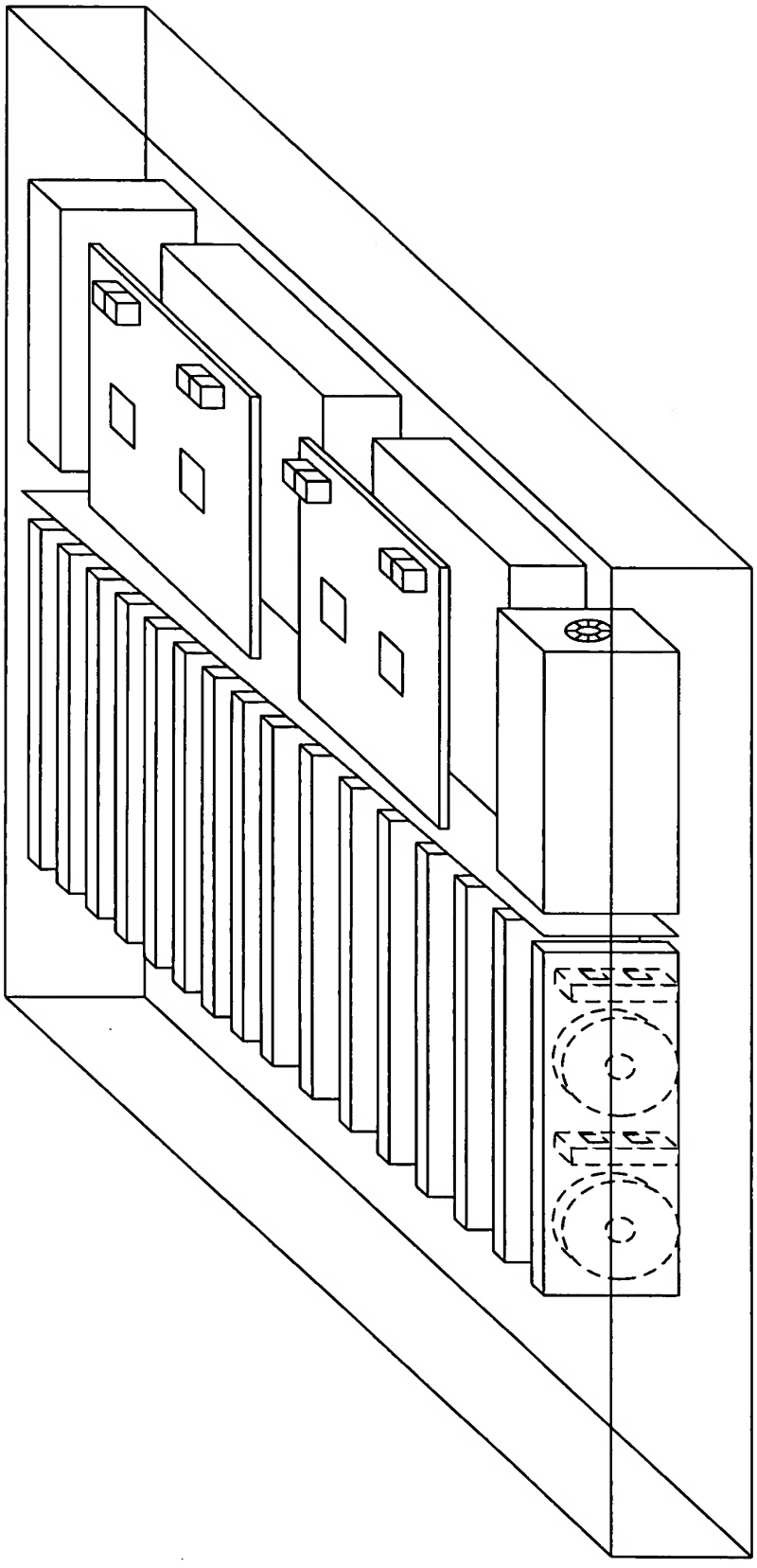


Figure 12

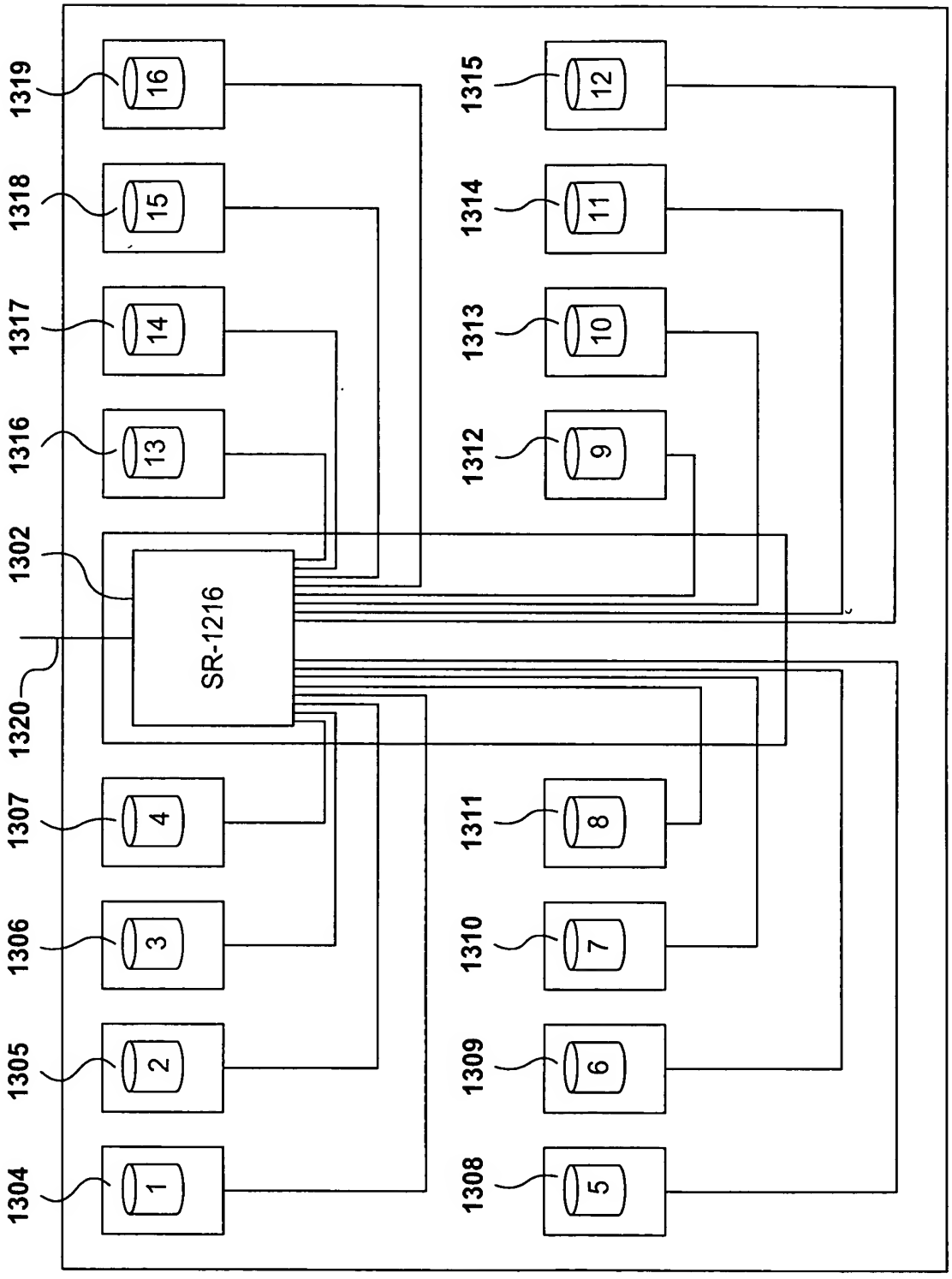

1319
16
1318
15
1317
14
1316
13
1315
12
1314
11
1313
10
1312
9
1302
SR-1216
1320
1307
4
1306
3
1305
2
1304
1
1311
8
1310
7
1309
6
1308
5

Figure 13A

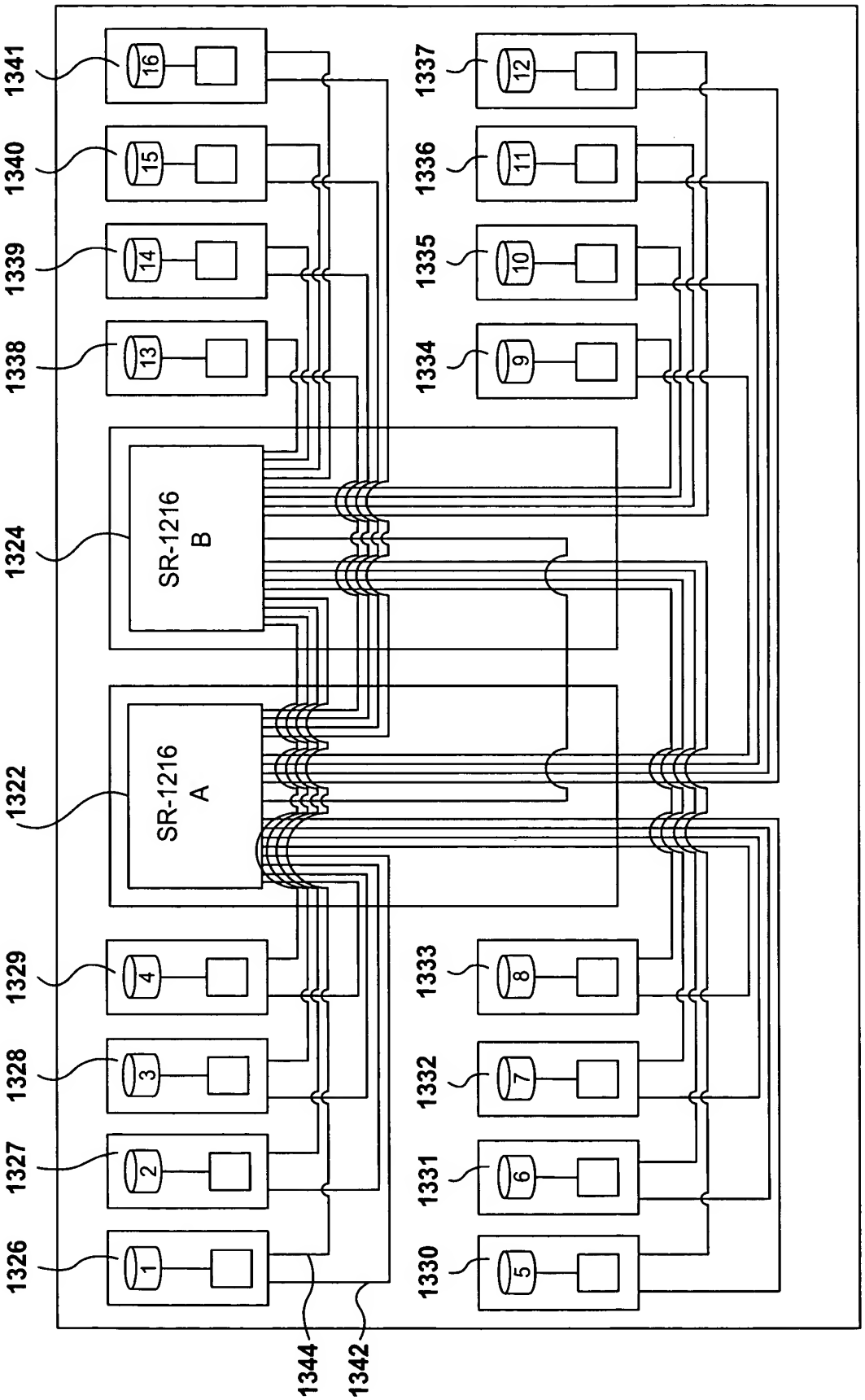

1341
1340
1339
1338
1337
1336
1335
1334
1324
SR-1216
B
1322
SR-1216
A
1329
1328
1327
1326
1333
1332
1331
1330
1344
1342

Figure 13B

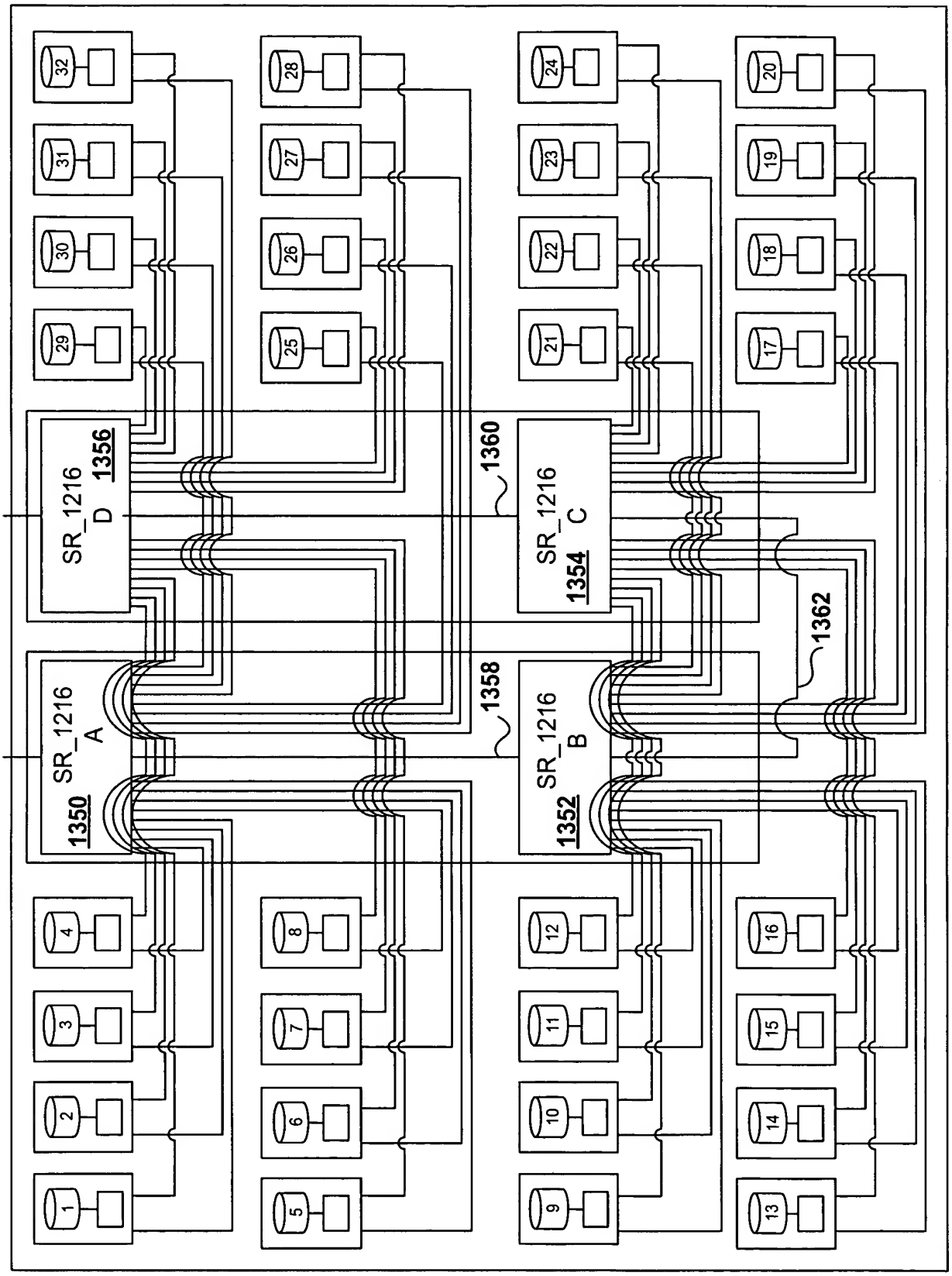

SR_1216 A
1350
SR_1216 B
1352
SR_1216 C
1354
SR_1216 D
1356
1358
1360
1362
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32

Figure 13C

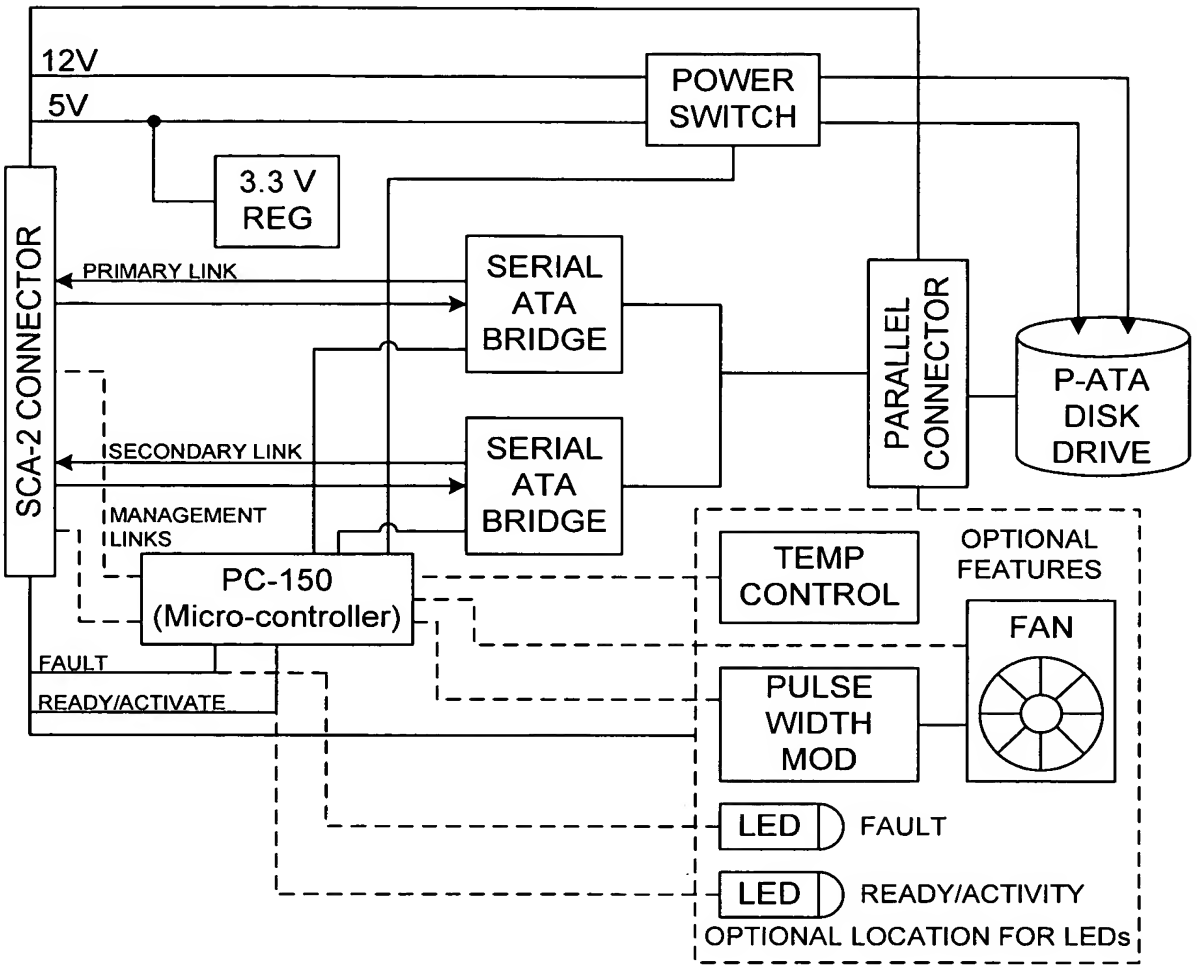

12V
5V
POWER SWITCH
3.3 V REG
SCA-2 CONNECTOR
PRIMARY LINK
SERIAL ATA BRIDGE
PARALLEL CONNECTOR
P-ATA DISK DRIVE
SECONDARY LINK
SERIAL ATA BRIDGE
MANAGEMENT LINKS
PC-150 (Micro-controller)
TEMP CONTROL
OPTIONAL FEATURES
FAN
FAULT
READY/ACTIVATE
PULSE WIDTH MOD
LED
FAULT
LED
READY/ACTIVITY
OPTIONAL LOCATION FOR LEDs

Figure 14A

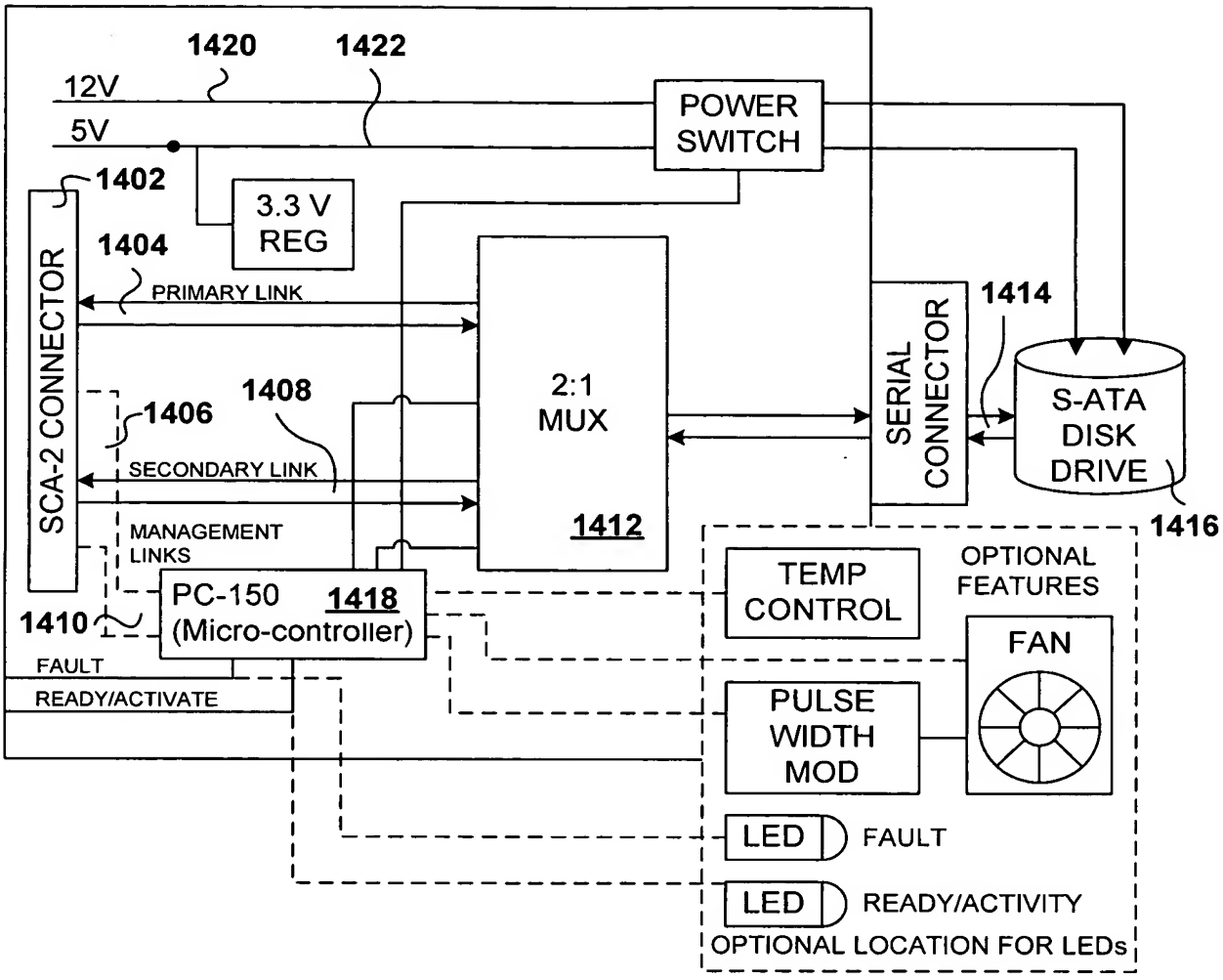

1420
1422
12V
5V
POWER SWITCH
1402
3.3 V REG
1404
PRIMARY LINK
SCA-2 CONNECTOR
1406
1408
SECONDARY LINK
MANAGEMENT LINKS
2:1 MUX
1412
SERIAL CONNECTOR
1414
S-ATA DISK DRIVE
1416
1410
PC-150 1418
(Micro-controller)
FAULT
READY/ACTIVATE
TEMP CONTROL
OPTIONAL FEATURES
FAN
PULSE WIDTH MOD
LED
FAULT
LED
READY/ACTIVITY
OPTIONAL LOCATION FOR LEDs

Figure 14B

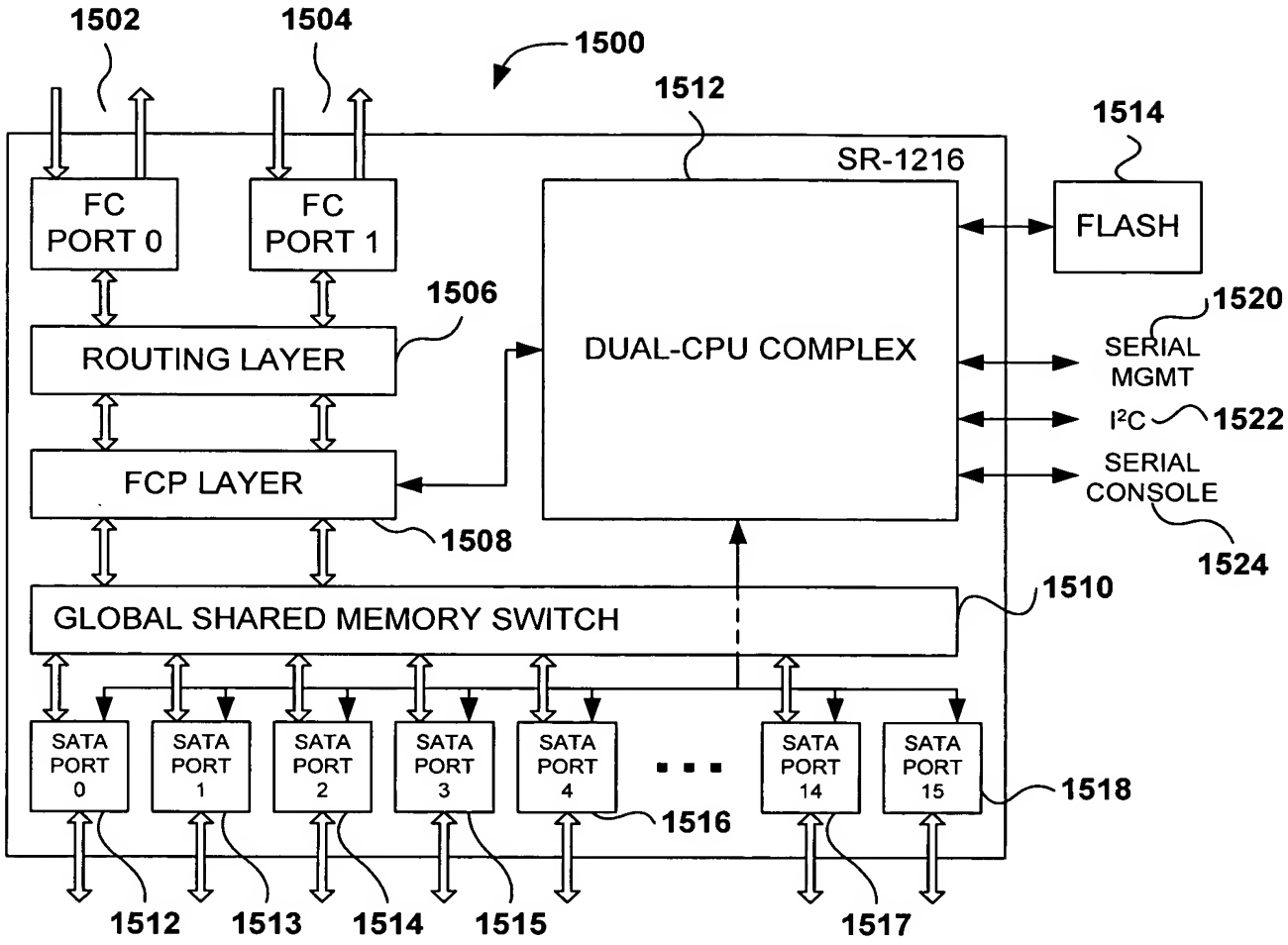

1502
1504
1500
1512
1514
SR-1216
FC PORT 0
FC PORT 1
FLASH
1506
1520
ROUTING LAYER
DUAL-CPU COMPLEX
SERIAL MGMT
I²C
1522
FCP LAYER
SERIAL CONSOLE
1508
1524
1510
GLOBAL SHARED MEMORY SWITCH
SATA PORT 0
SATA PORT 1
SATA PORT 2
SATA PORT 3
SATA PORT 4
SATA PORT 14
SATA PORT 15
1518
1516
1512
1513
1514
1515
1517

Figure 15

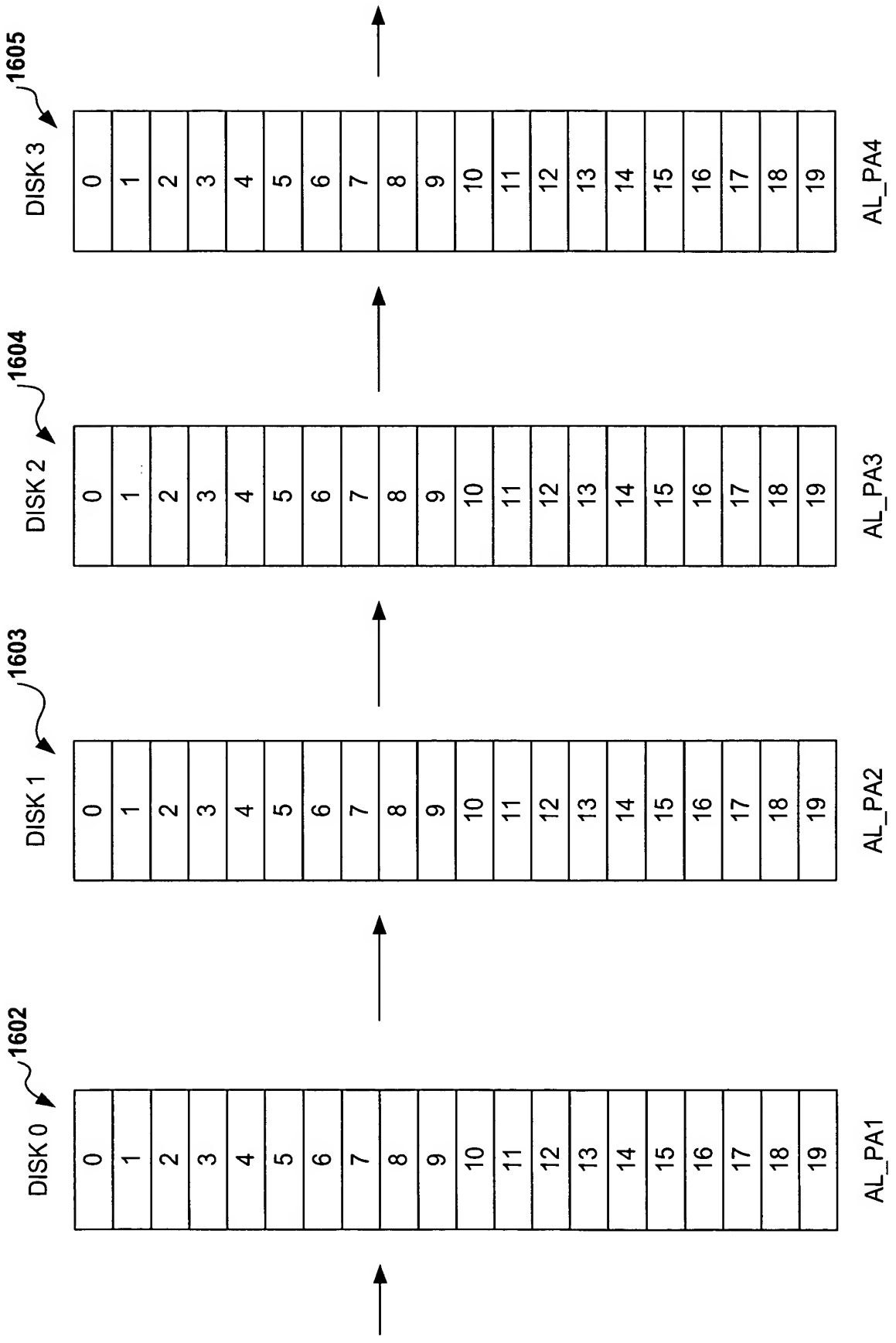

DISK 0
1602
DISK 1
1603
DISK 2
1604
DISK 3
1605
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
AL_PA1
AL_PA2
AL_PA3
AL_PA4

Figure 16A

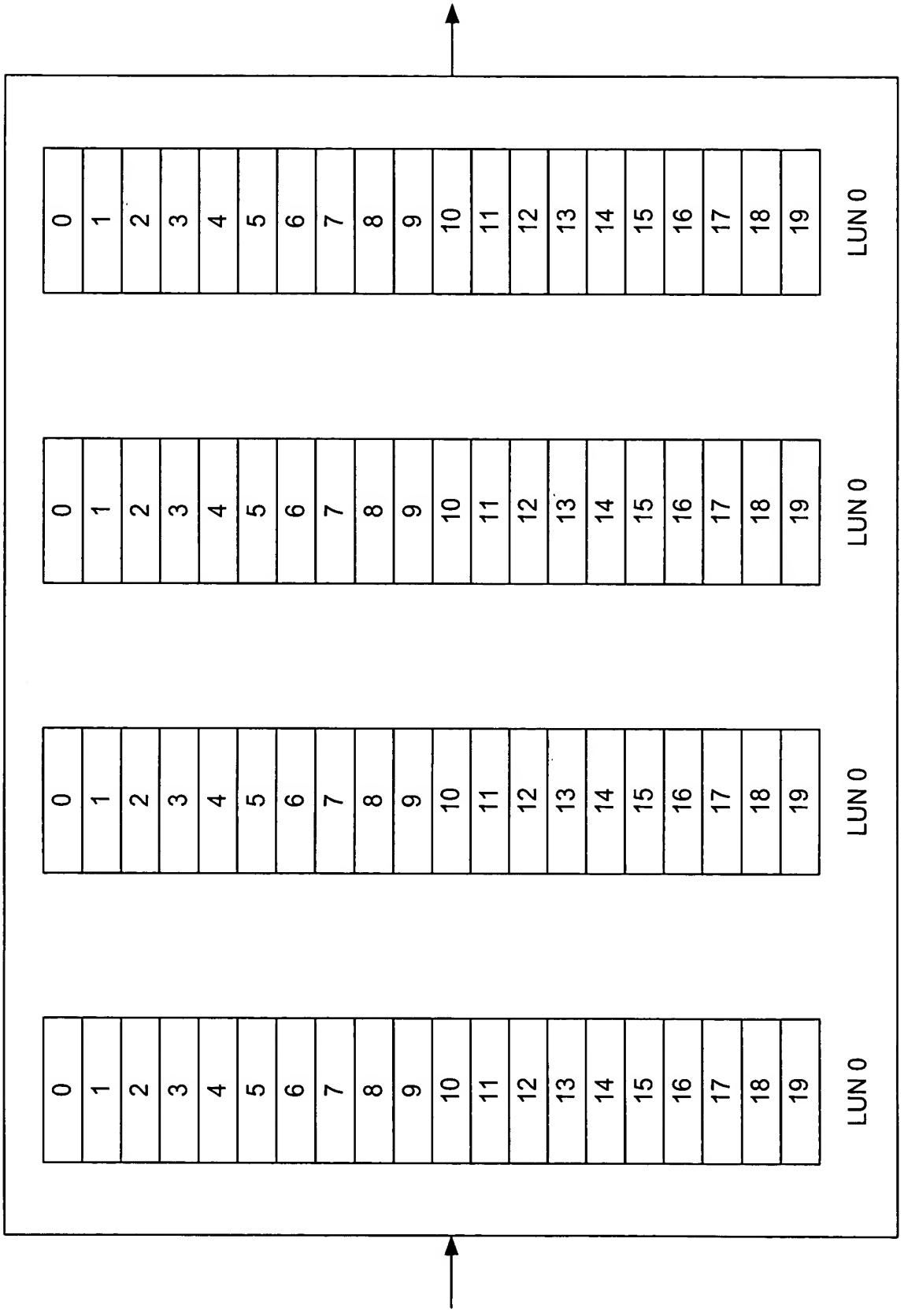

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
LUN 0
AL_PA1
AL_PA2
AL_PA3
AL_PA4

Figure 16B

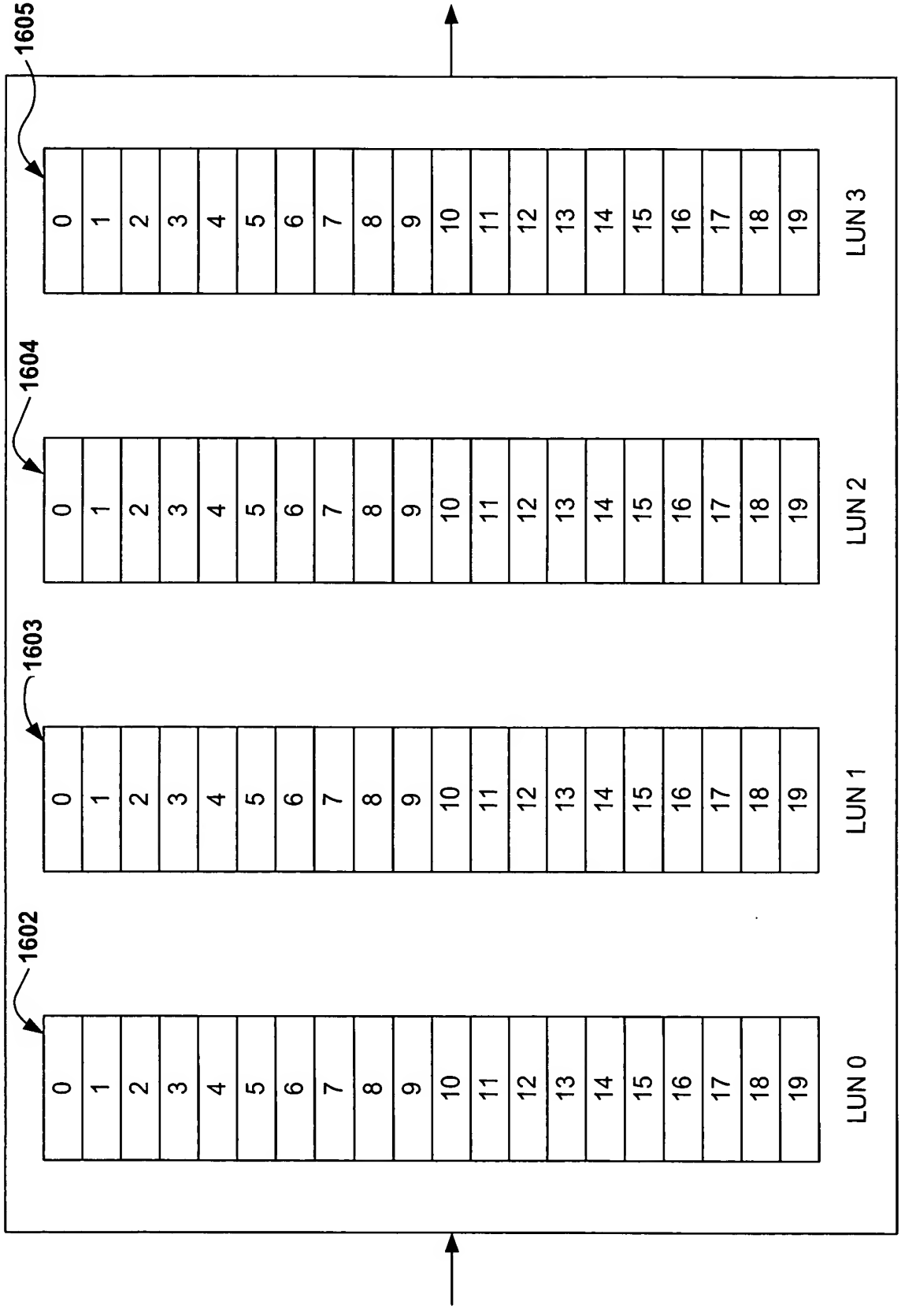

1605
1604
1603
1602
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
LUN 3
LUN 2
LUN 1
LUN 0
AL_PA1

Figure 16C

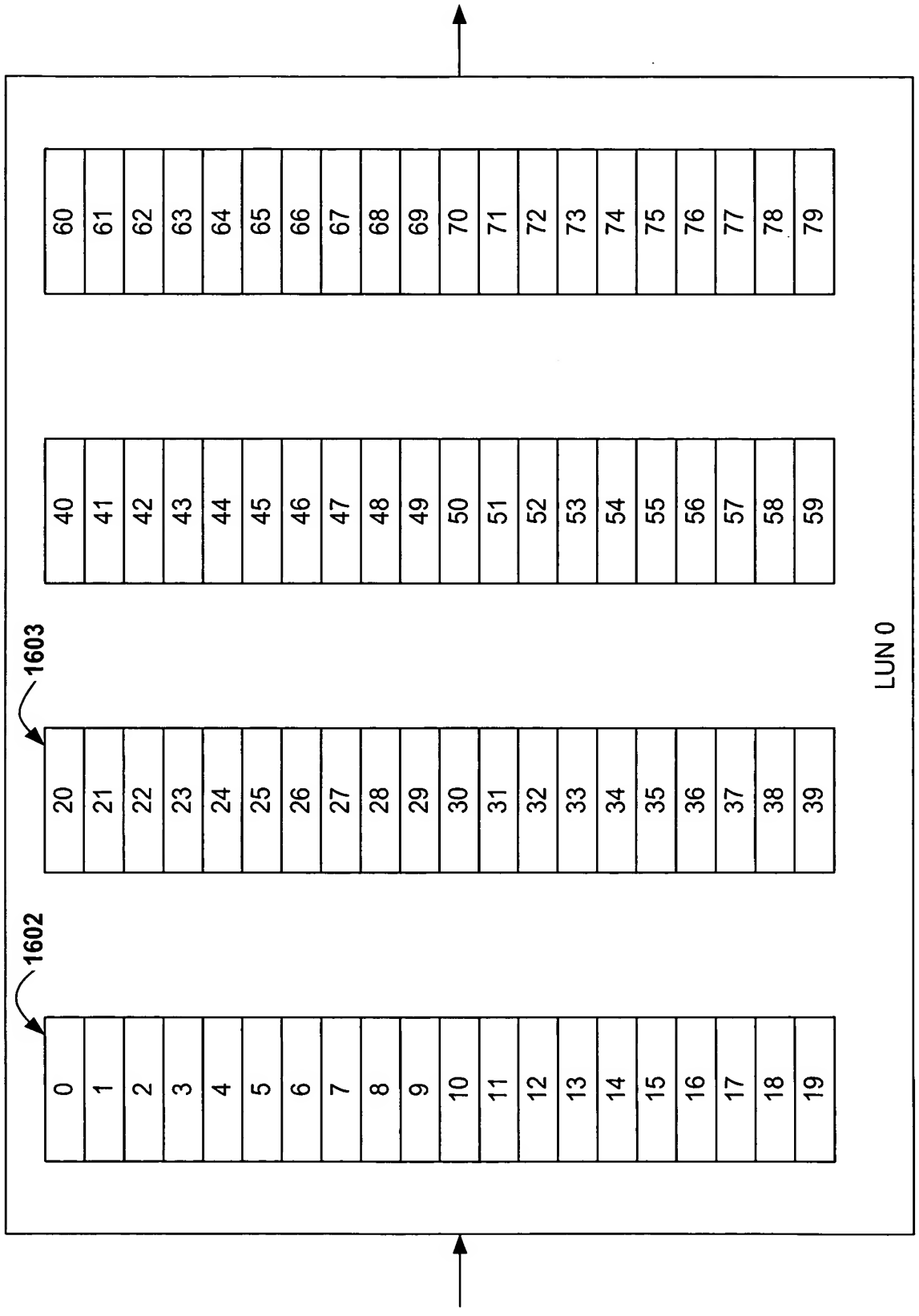

1602
1603
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59
60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79
LUN 0
AL_PA1

Figure 16D

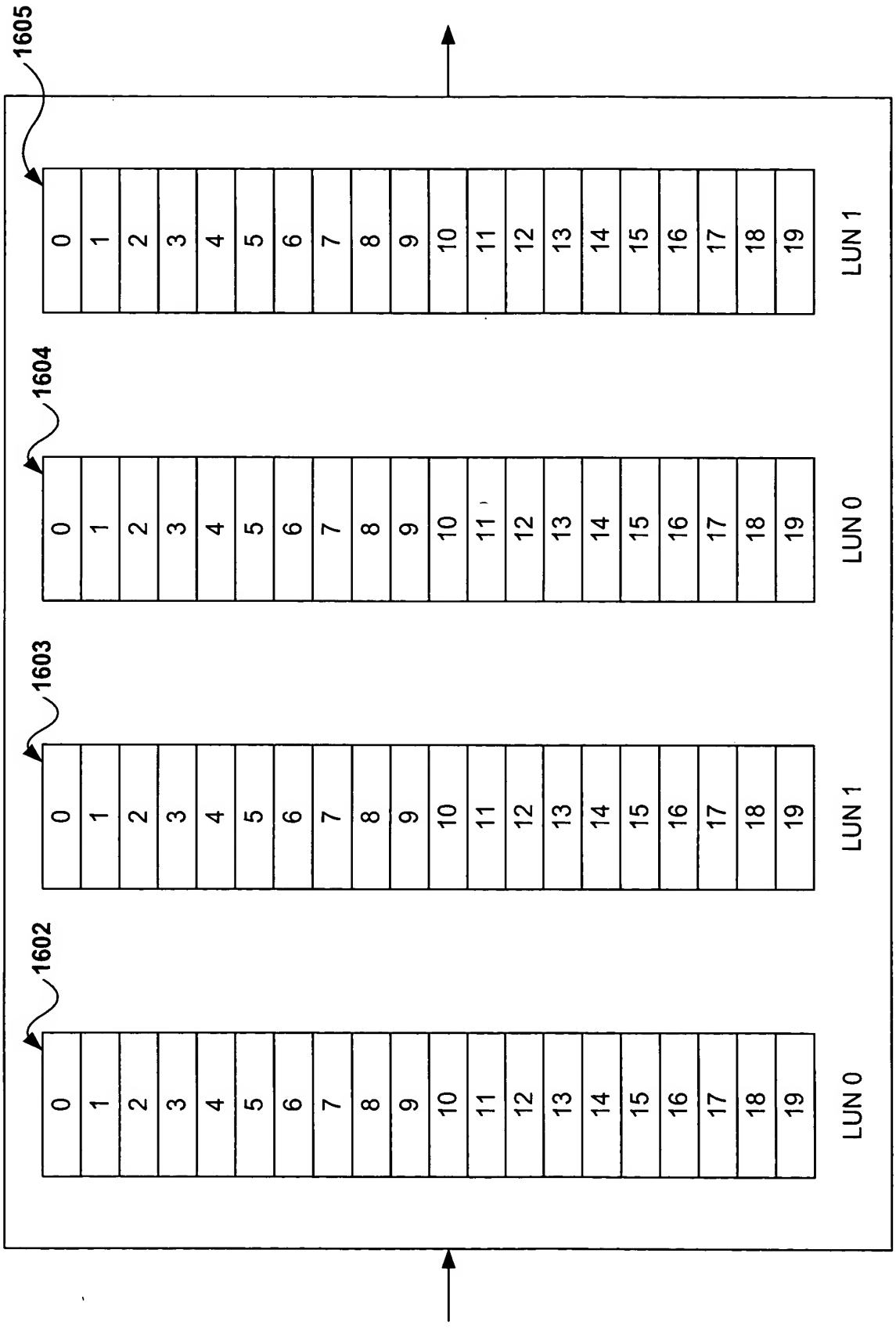

1605
1604
1603
1602
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
LUN 1
LUN 0
LUN 1
LUN 0
AL_PA2
AL_PA1

Figure 16E

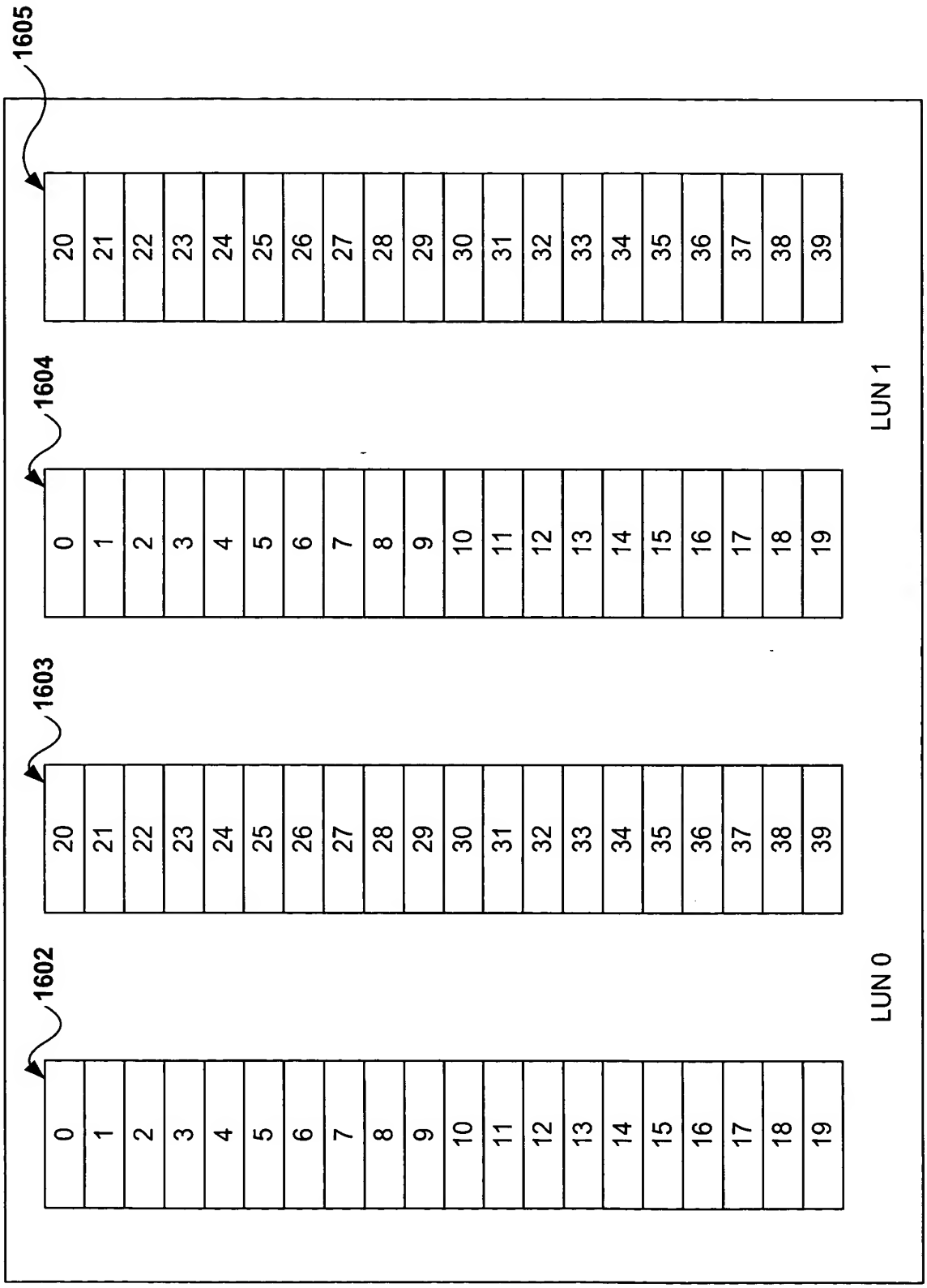

1605
1604
1603
1602
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
LUN 0
LUN 1
AL_PA1
AL_PA2

Figure 16F

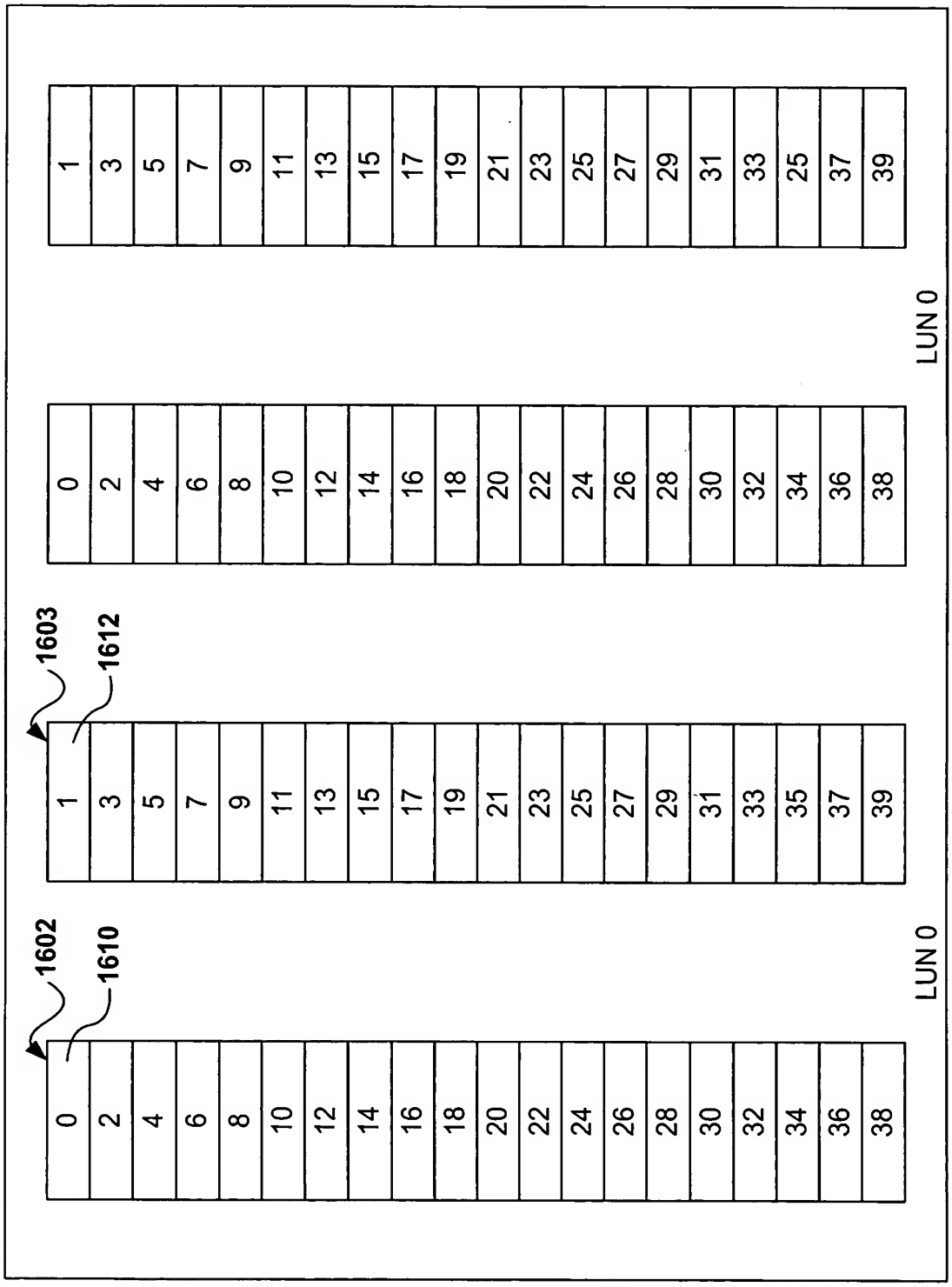

1602
1610
1603
1612
0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38
1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39
0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38
1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 25 37 39
LUN 0
LUN 0
AL_PA1
AL_PA2

Figure 16G

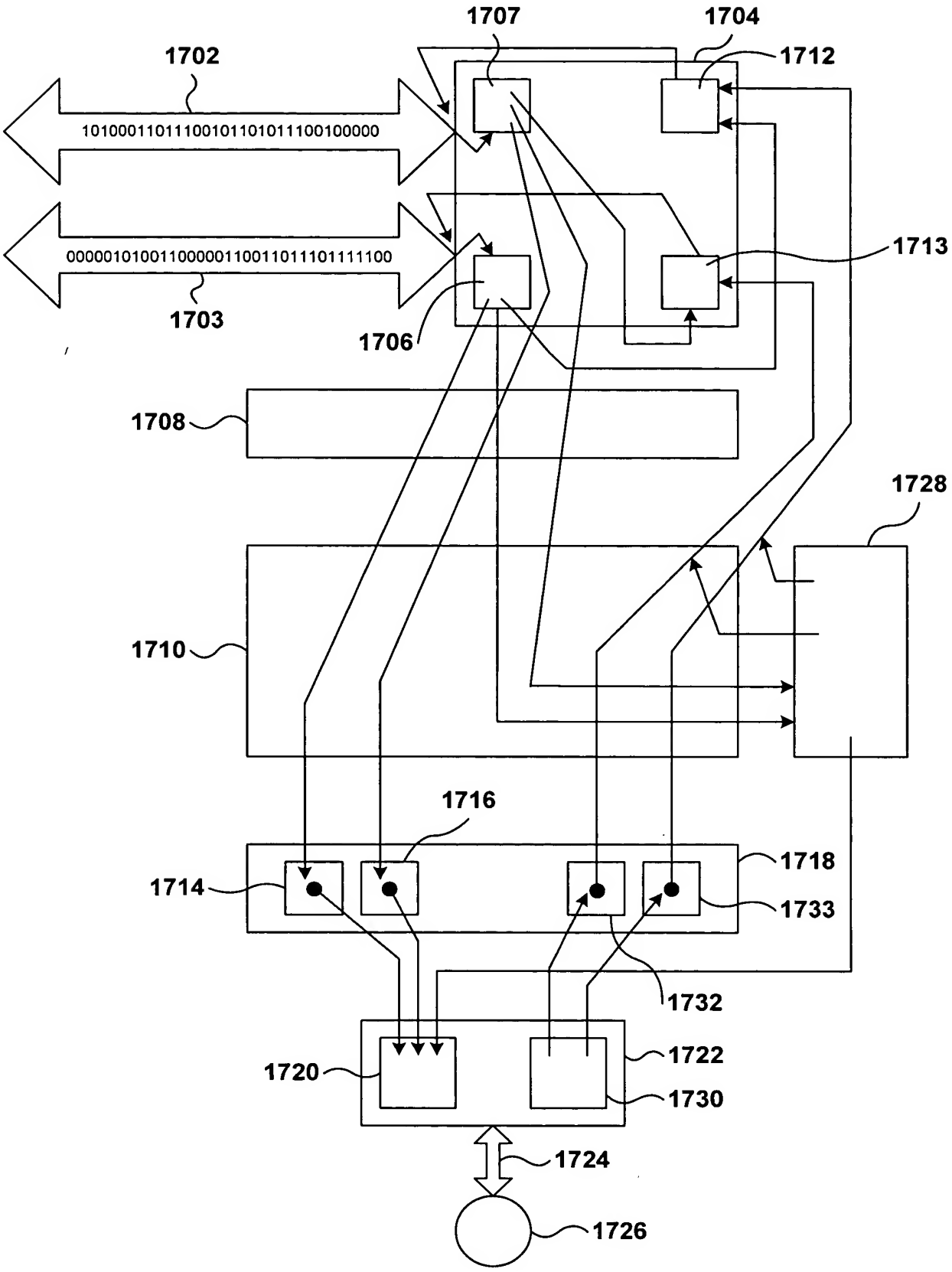

1707
1704
1702
1712
1010001101110010110101110010000
0
0000010100110000011001101110111100
1713
1703
1706
1708
1728
1710
1716
1718
1714
1733
1732
1720
1722
1730
1724
1726

Figure 17A

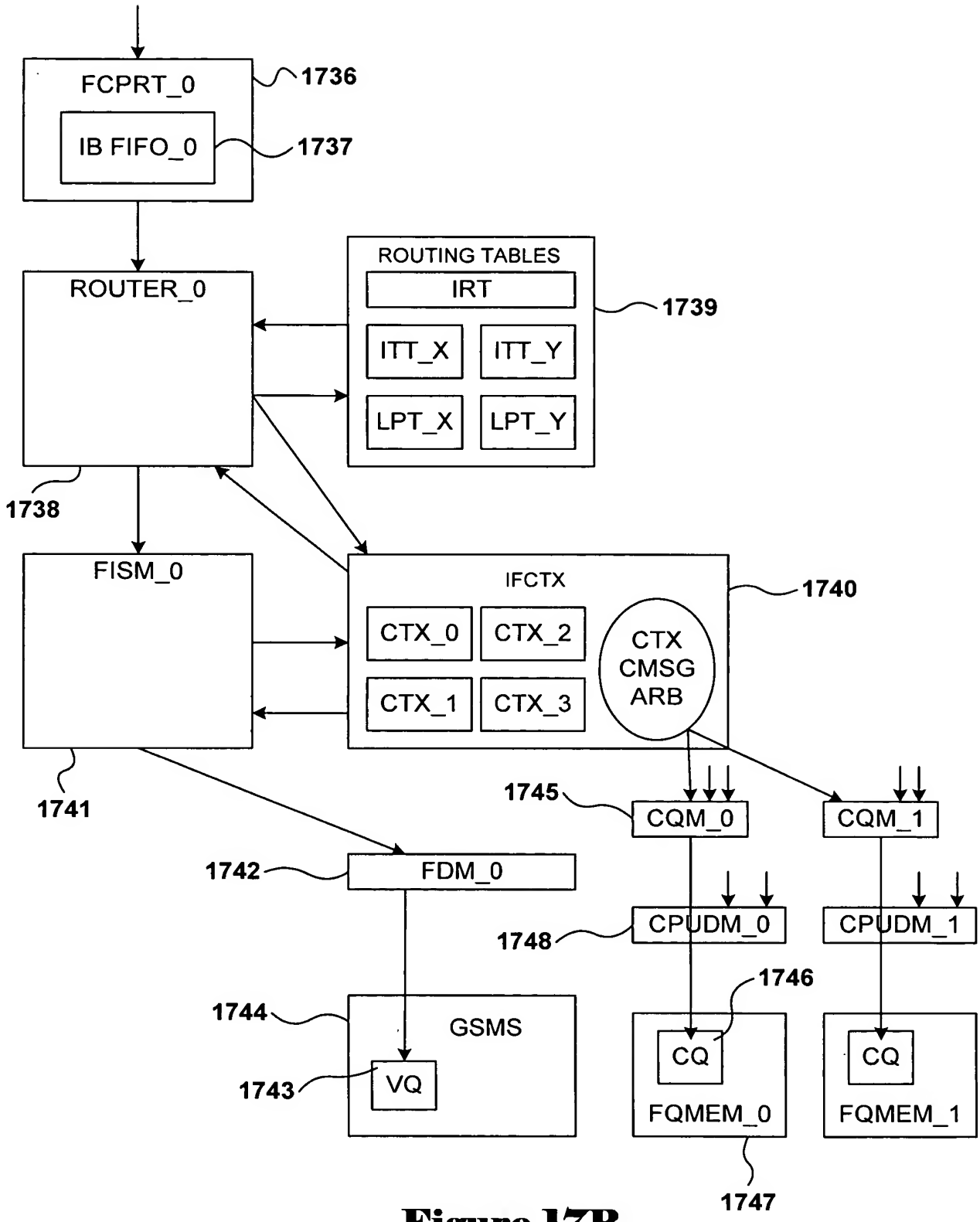

FCPRT_0
1736
IB FIFO_0
1737
ROUTING TABLES
IRT
1739
ITT_X
ITT_Y
LPT_X
LPT_Y
ROUTER_0
1738
FISM_0
IFCTX
1740
CTX_0
CTX_2
CTX_1
CTX_3
CTX CMSG ARB
1741
1745
CQM_0
CQM_1
1742
FDM_0
CPUDM_0
CPUDM_1
1748
1746
1744
GSMS
CQ
CQ
1743
VQ
FQMEM_0
FQMEM_1
1747

Figure 17B

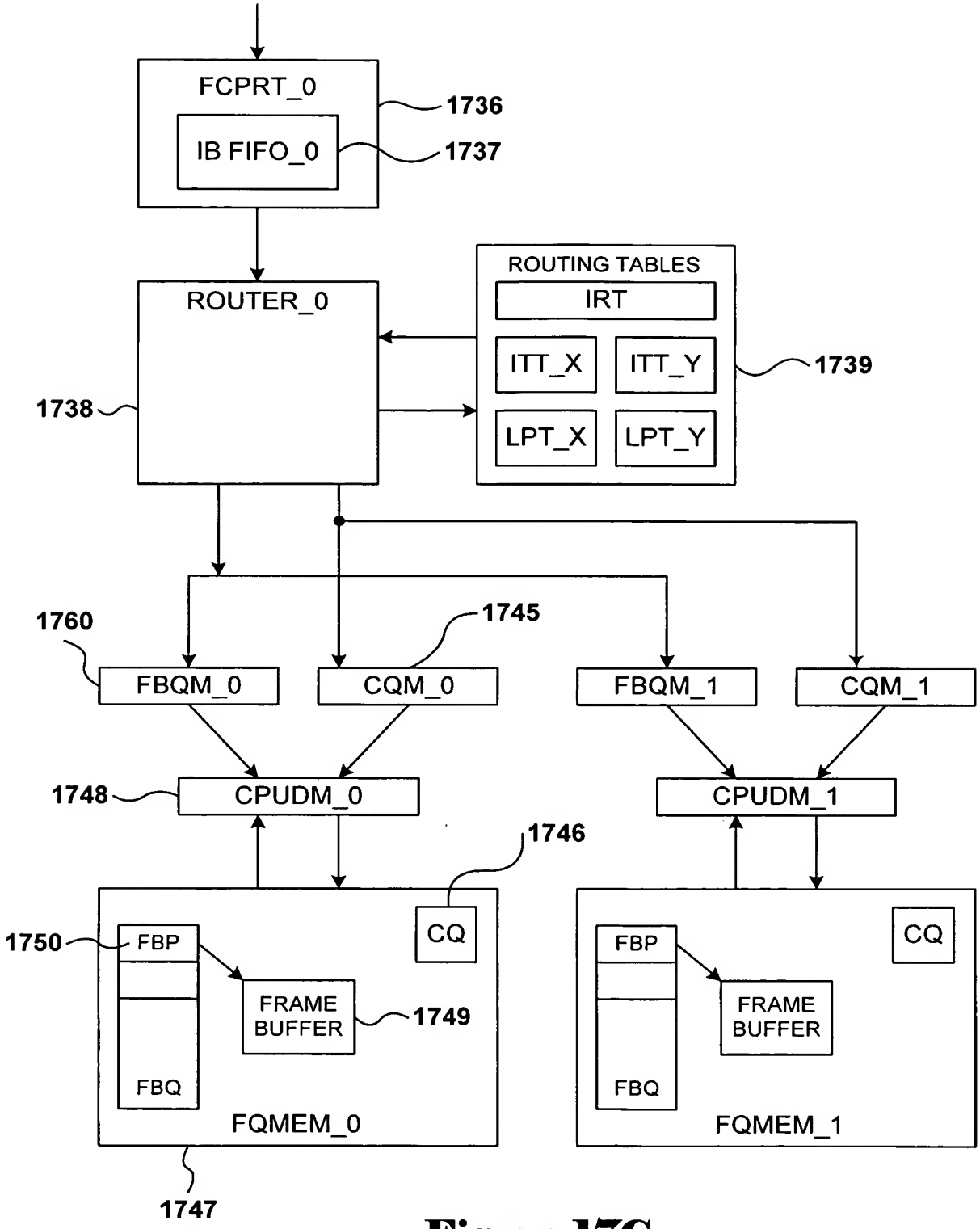

FCPRT_0
1736
IB FIFO_0
1737
ROUTING TABLES
IRT
ROUTER_0
ITT_X
ITT_Y
1739
1738
LPT_X
LPT_Y
1760
1745
FBQM_0
CQM_0
FBQM_1
CQM_1
1748
CPUDM_0
CPUDM_1
1746
CQ
CQ
1750
FBP
FBP
FRAME BUFFER
1749
FRAME BUFFER
FBQ
FBQ
FQMEM_0
FQMEM_1
1747

Figure 17C

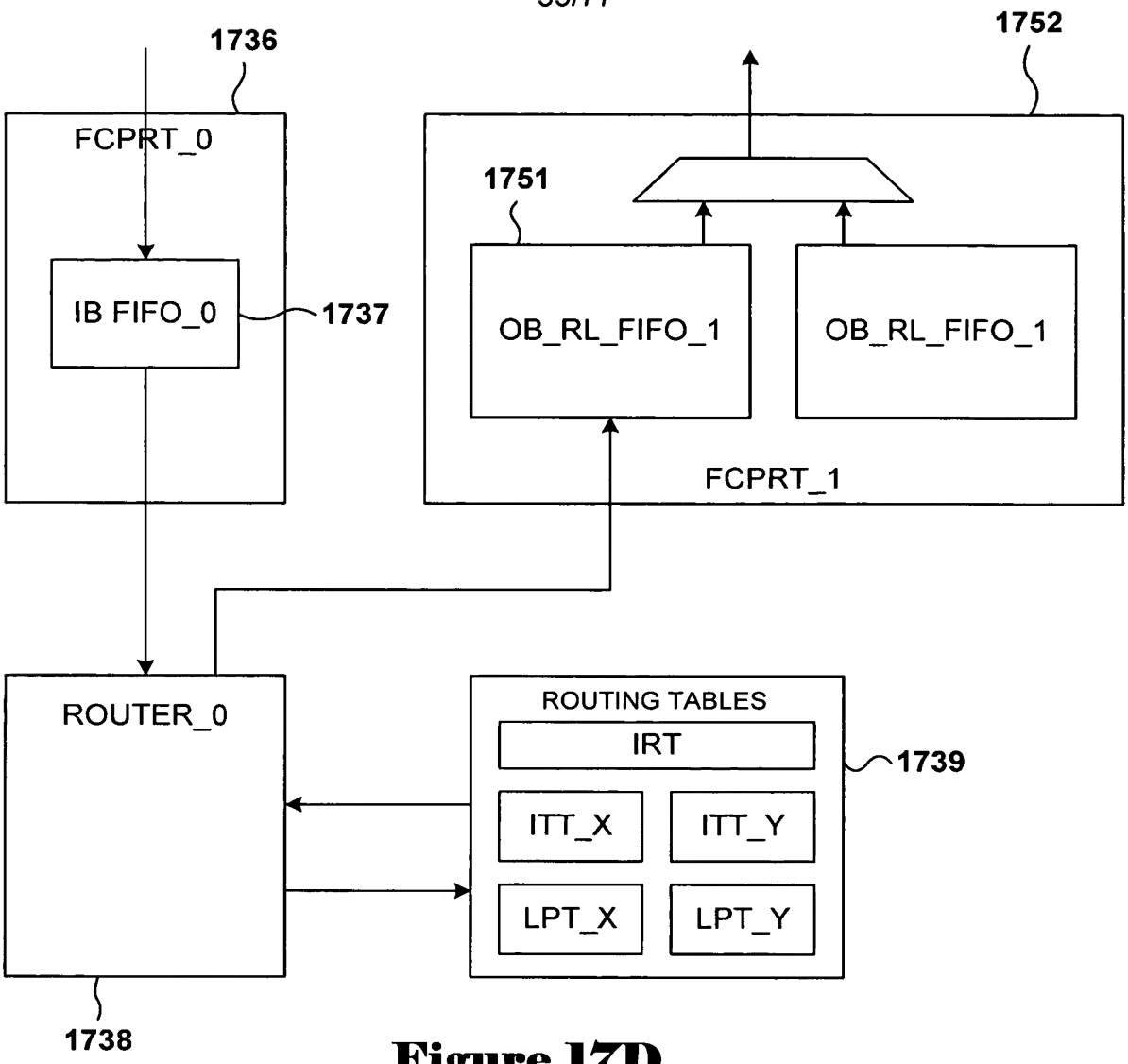

1736
FCPRT_0
IB FIFO_0
1737
1752
1751
OB_RL_FIFO_1
OB_RL_FIFO_1
FCPRT_1
ROUTER_0
ROUTING TABLES
IRT
1739
ITT_X
ITT_Y
LPT_X
LPT_Y
1738

Figure 17D

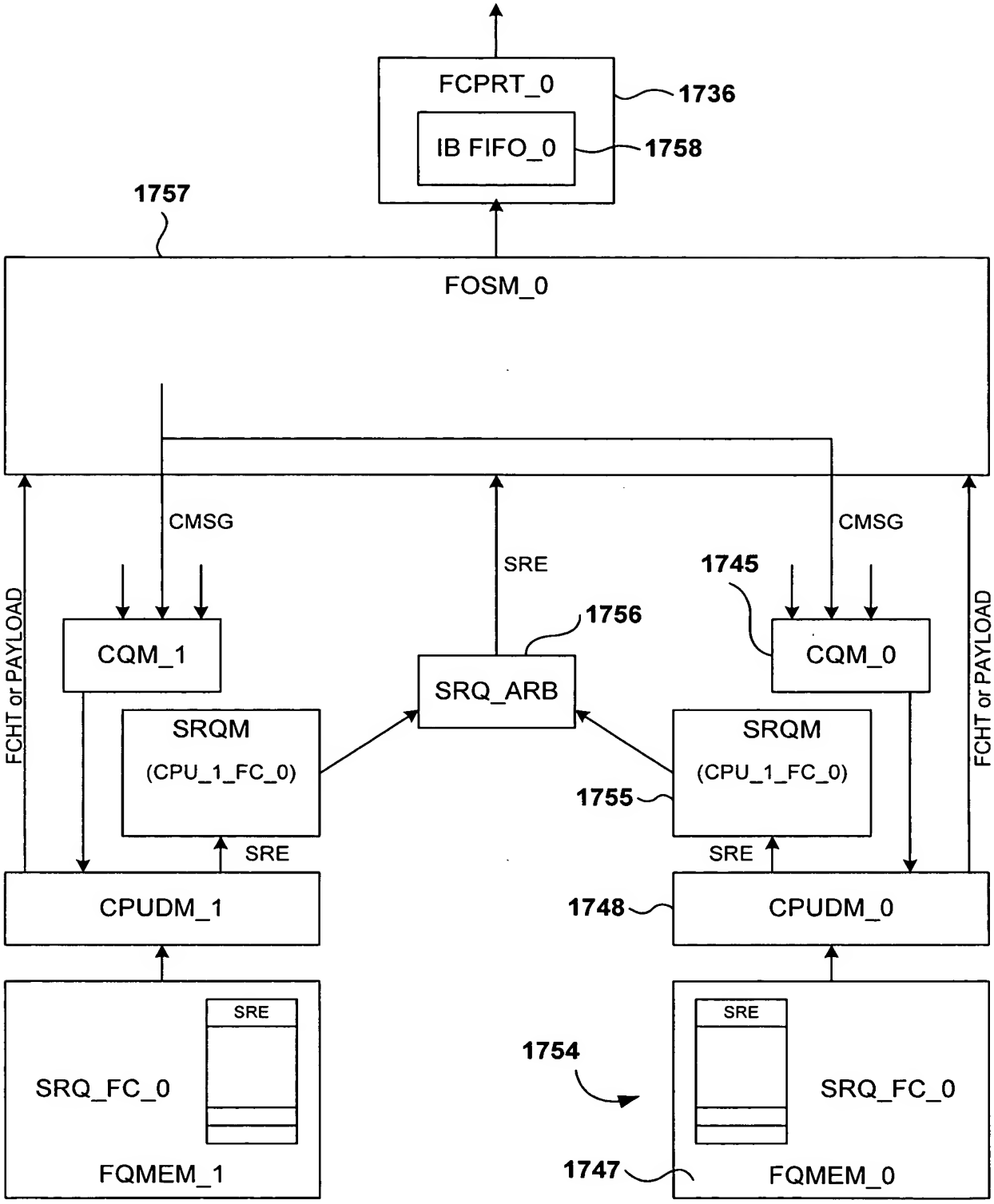

FCPRT_0
1736
IB FIFO_0
1758
1757
FOSM_0
CMSG
SRE
CMSG
1745
1756
FCHT or PAYLOAD
CQM_1
SRQ_ARB
CQM_0
FCHT or PAYLOAD
SRQM
(CPU_1_FC_0)
SRQM
(CPU_1_FC_0)
1755
SRE
SRE
CPUDM_1
1748
CPUDM_0
SRE
SRE
1754
SRQ_FC_0
SRQ_FC_0
1747
FQMEM_1
FQMEM_0

Figure 17E

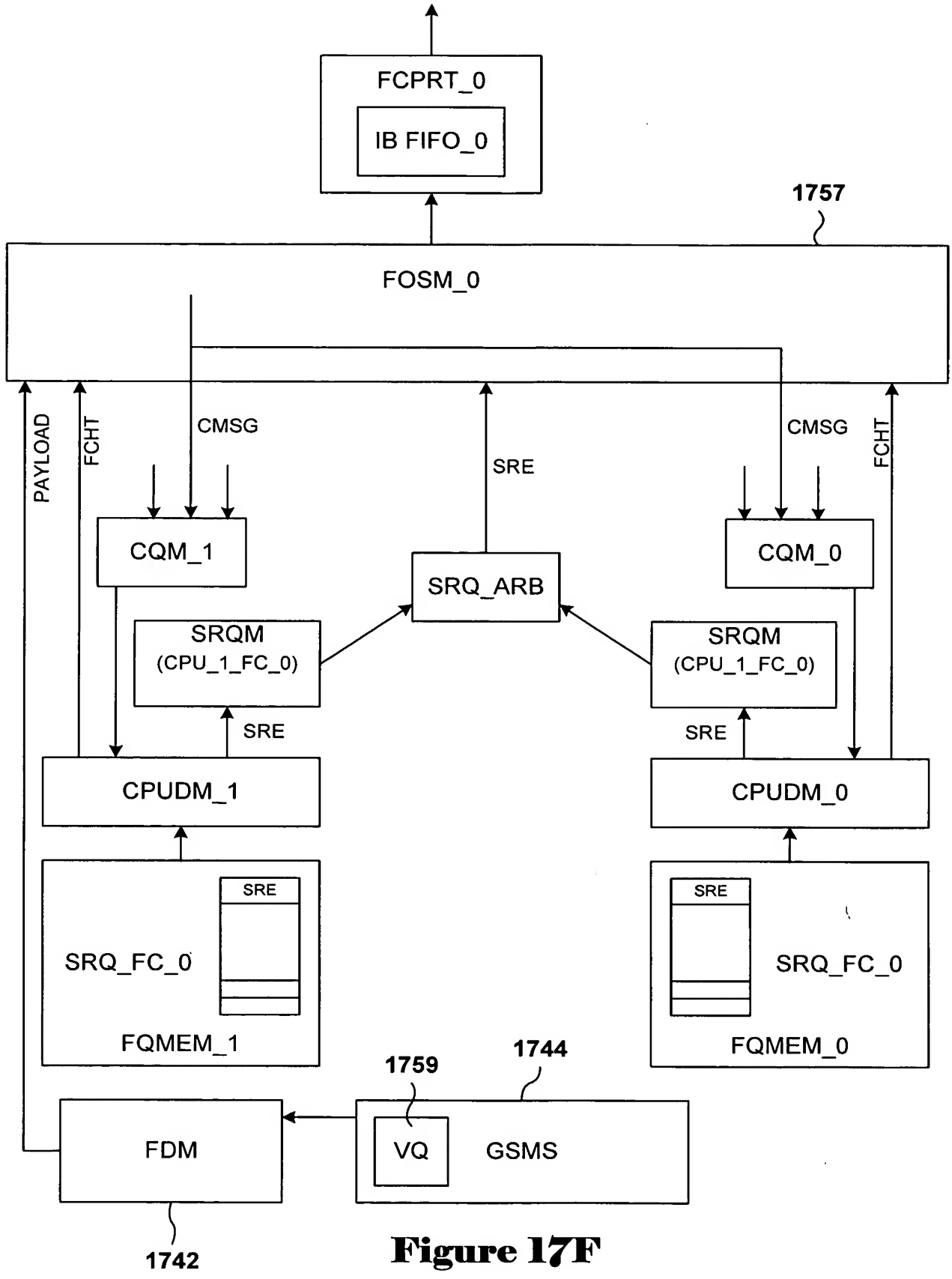

FCPRT_0
IB FIFO_0
1757
FOSM_0
PAYLOAD
FCHT
CMSG
SRE
CMSG
FCHT
CQM_1
SRQ_ARB
CQM_0
SRQM
(CPU_1_FC_0)
SRQM
(CPU_1_FC_0)
SRE
SRE
CPUDM_1
CPUDM_0
SRE
SRE
SRQ_FC_0
SRQ_FC_0
FQMEM_1
FQMEM_0
1759
1744
FDM
VQ
GSMS
1742

Figure 17F

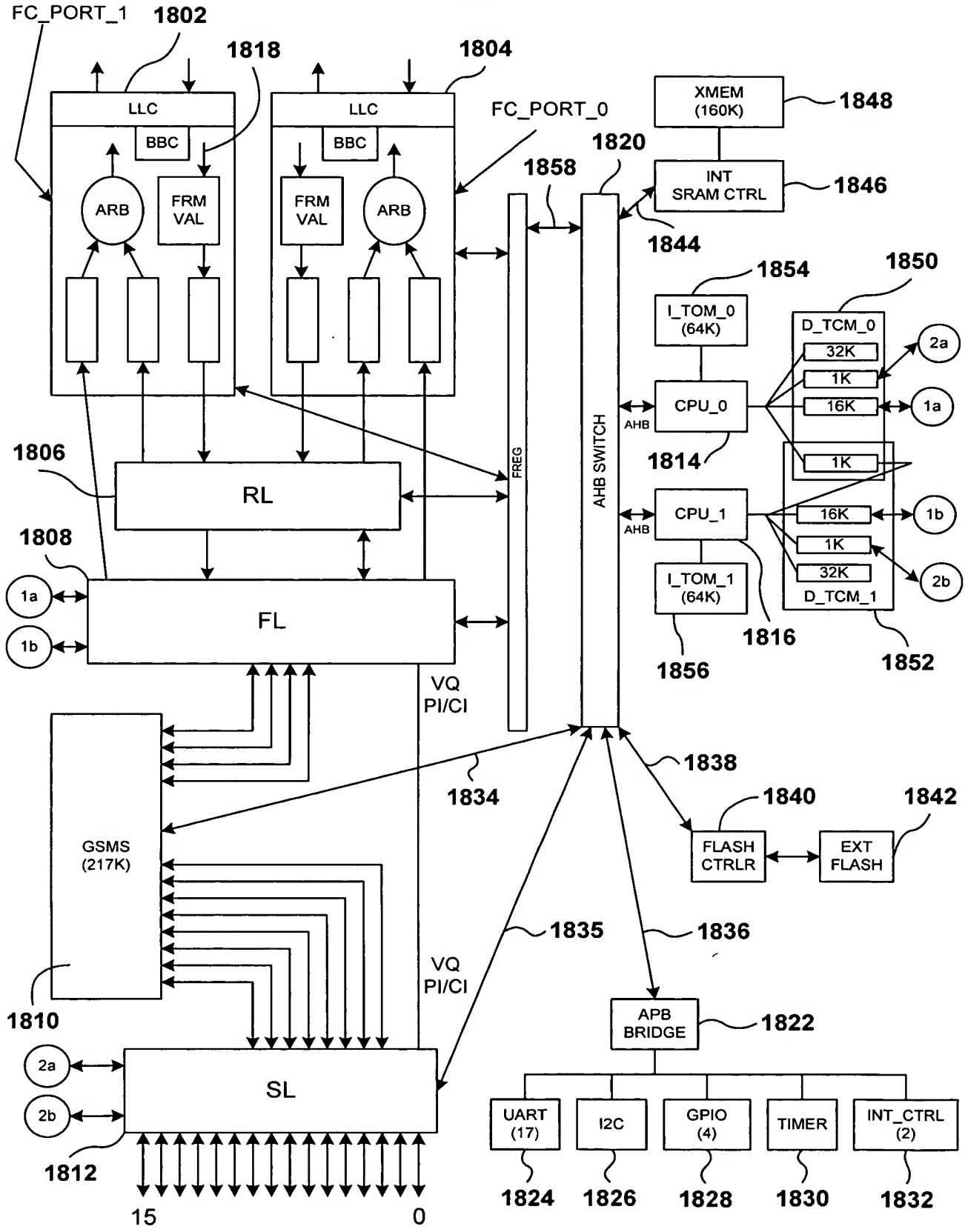

FC_PORT_1
1802
1818
1804
LLC
BBC
ARB
FRM VAL
LLC
BBC
FRM VAL
ARB
FC_PORT_0
1820
1858
XMEM (160K)
1848
INT SRAM CTRL
1846
1844
1854
1850
I_TOM_0 (64K)
D_TCM_0
32K
1K
16K
2a
1a
CPU_0
AHB
1814
1806
RL
FREG
AHB SWITCH
1K
CPU_1
AHB
16K
1K
32K
1b
2b
1808
1a
1b
FL
I_TOM_1 (64K)
D_TCM_1
1816
1856
1852
VQ PI/CI
1834
1838
1840
1842
FLASH CTRLR
EXT FLASH
GSMS (217K)
1835
1836
VQ PI/CI
1810
APB BRIDGE
1822
2a
2b
SL
UART (17)
I2C
GPIO (4)
TIMER
INT_CTRL (2)
1812
1824
1826
1828
1830
1832
15
0

Figure 18

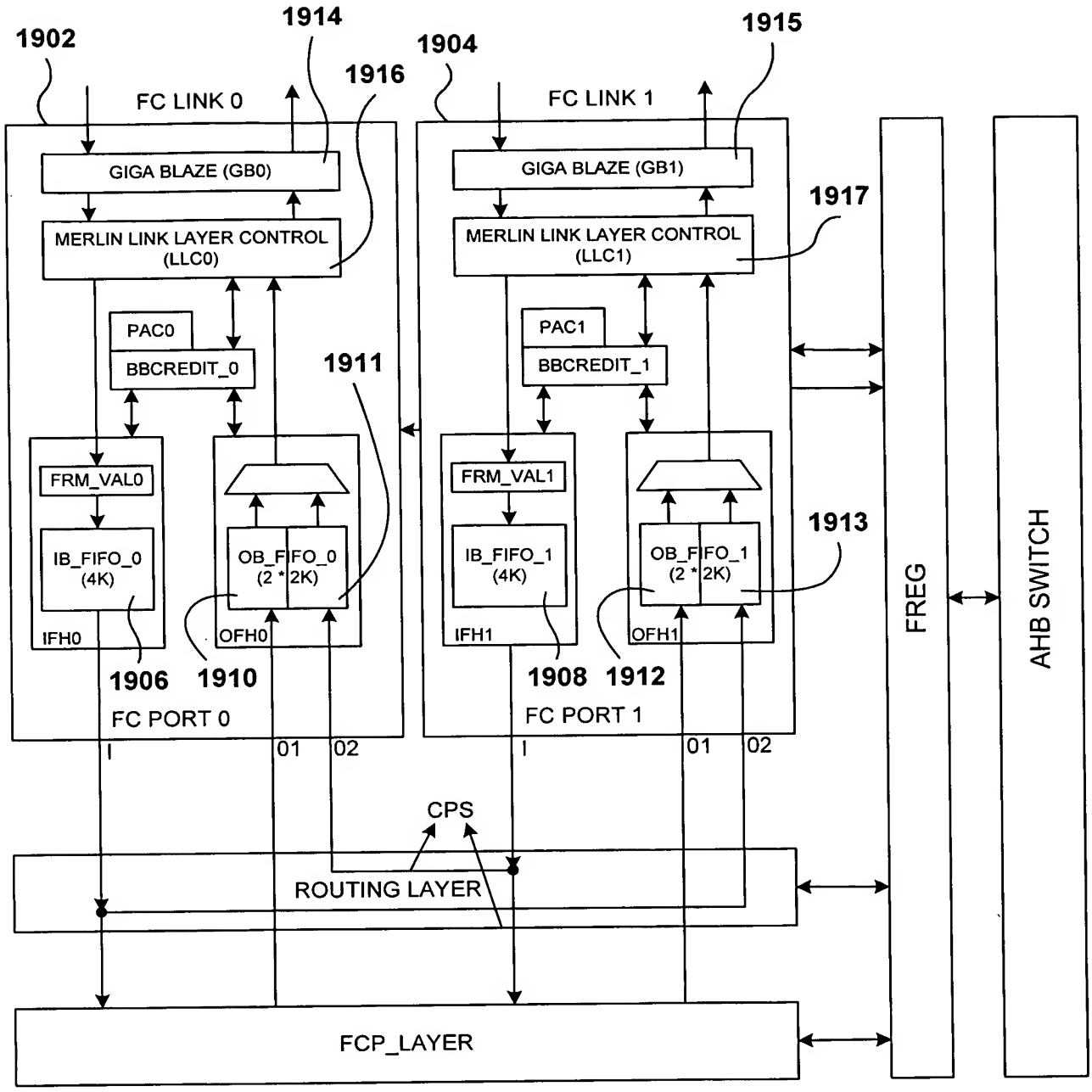

1902
1914
1904
1915
1916
FC LINK 0
FC LINK 1
GIGA BLAZE (GB0)
GIGA BLAZE (GB1)
1917
MERLIN LINK LAYER CONTROL (LLC0)
MERLIN LINK LAYER CONTROL (LLC1)
PAC0
BBCREDIT_0
PAC1
BBCREDIT_1
1911
FRM_VAL0
FRM_VAL1
IB_FIFO_0 (4K)
OB_FIFO_0 (2 * 2K)
IB_FIFO_1 (4K)
OB_FIFO_1 (2 * 2K)
1913
IFH0
OFH0
IFH1
OFH1
1906
1910
1908
1912
FC PORT 0
FC PORT 1
I
01
02
I
01
02
FREG
AHB SWITCH
CPS
ROUTING LAYER
FCP_LAYER

Figure 19

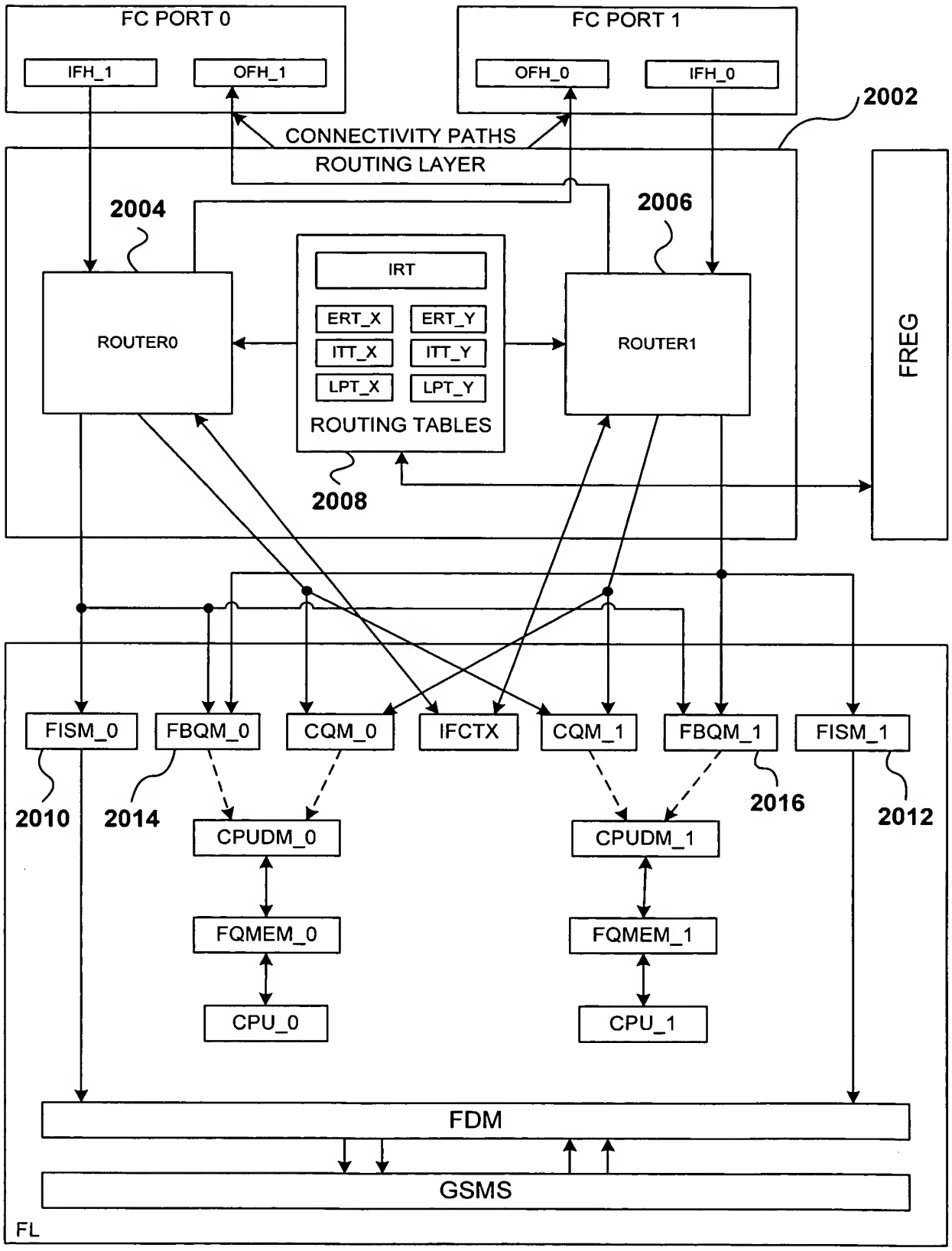

FC PORT 0
IFH_1
OFH_1
FC PORT 1
OFH_0
IFH_0
2002
CONNECTIVITY PATHS
ROUTING LAYER
2004
2006
IRT
ERT_X
ERT_Y
ITT_X
ITT_Y
LPT_X
LPT_Y
ROUTING TABLES
ROUTER0
ROUTER1
FREG
2008
FISM_0
FBQM_0
CQM_0
IFCTX
CQM_1
FBQM_1
FISM_1
2010
2014
2016
2012
CPUDM_0
CPUDM_1
FQMEM_0
FQMEM_1
CPU_0
CPU_1
FDM
GSMS
FL

Figure 20

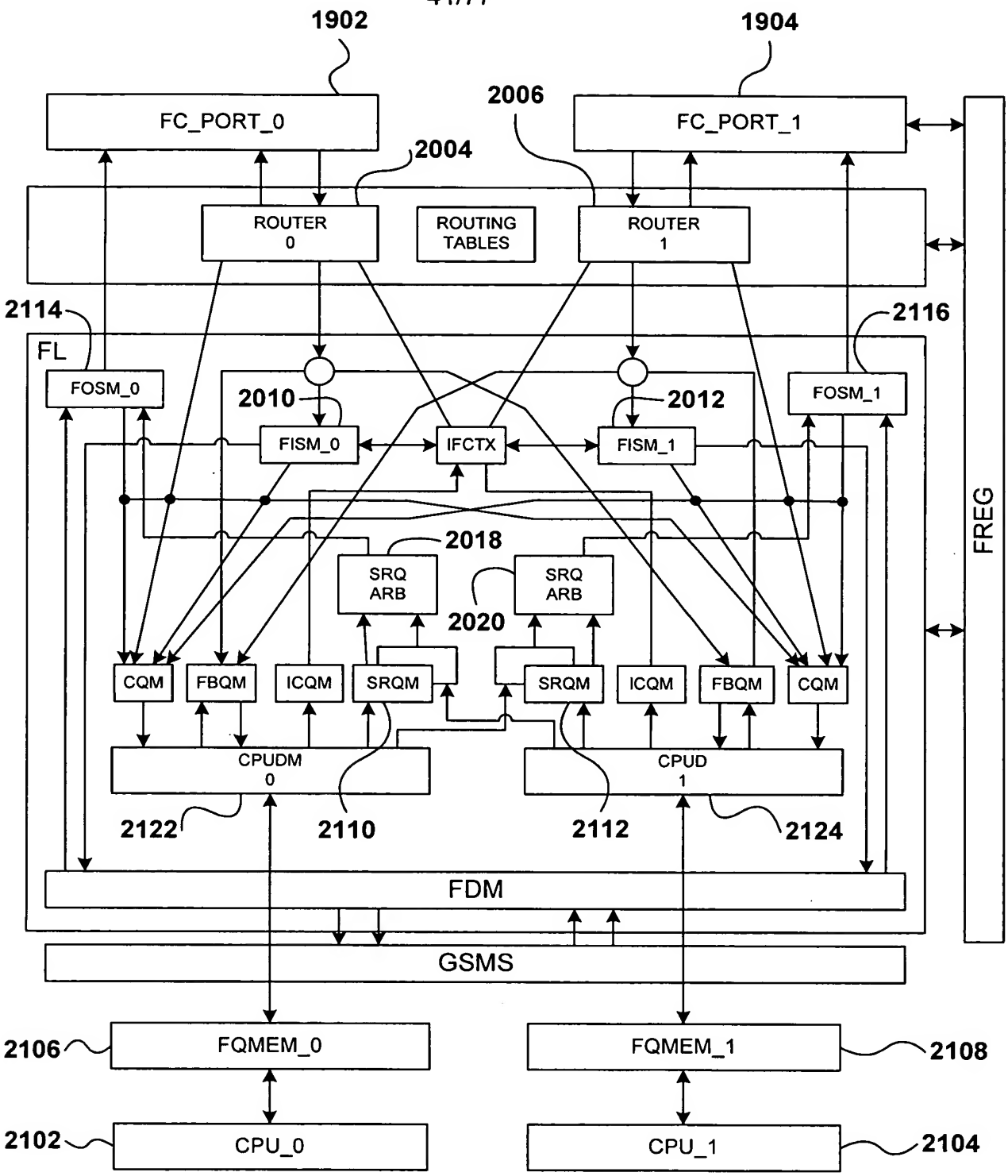

1902
1904
2006
FC_PORT_0
FC_PORT_1
2004
ROUTER 0
ROUTING TABLES
ROUTER 1
2114
2116
FL
FOSM_0
FOSM_1
2010
2012
FISM_0
IFCTX
FISM_1
FREG
2018
SRQ ARB
SRQ ARB
2020
CQM
FBQM
ICQM
SRQM
SRQM
ICQM
FBQM
CQM
CPUDM 0
CPUD 1
2122
2110
2112
2124
FDM
GSMS
2106
FQMEM_0
FQMEM_1
2108
2102
CPU_0
CPU_1
2104

Figure 21

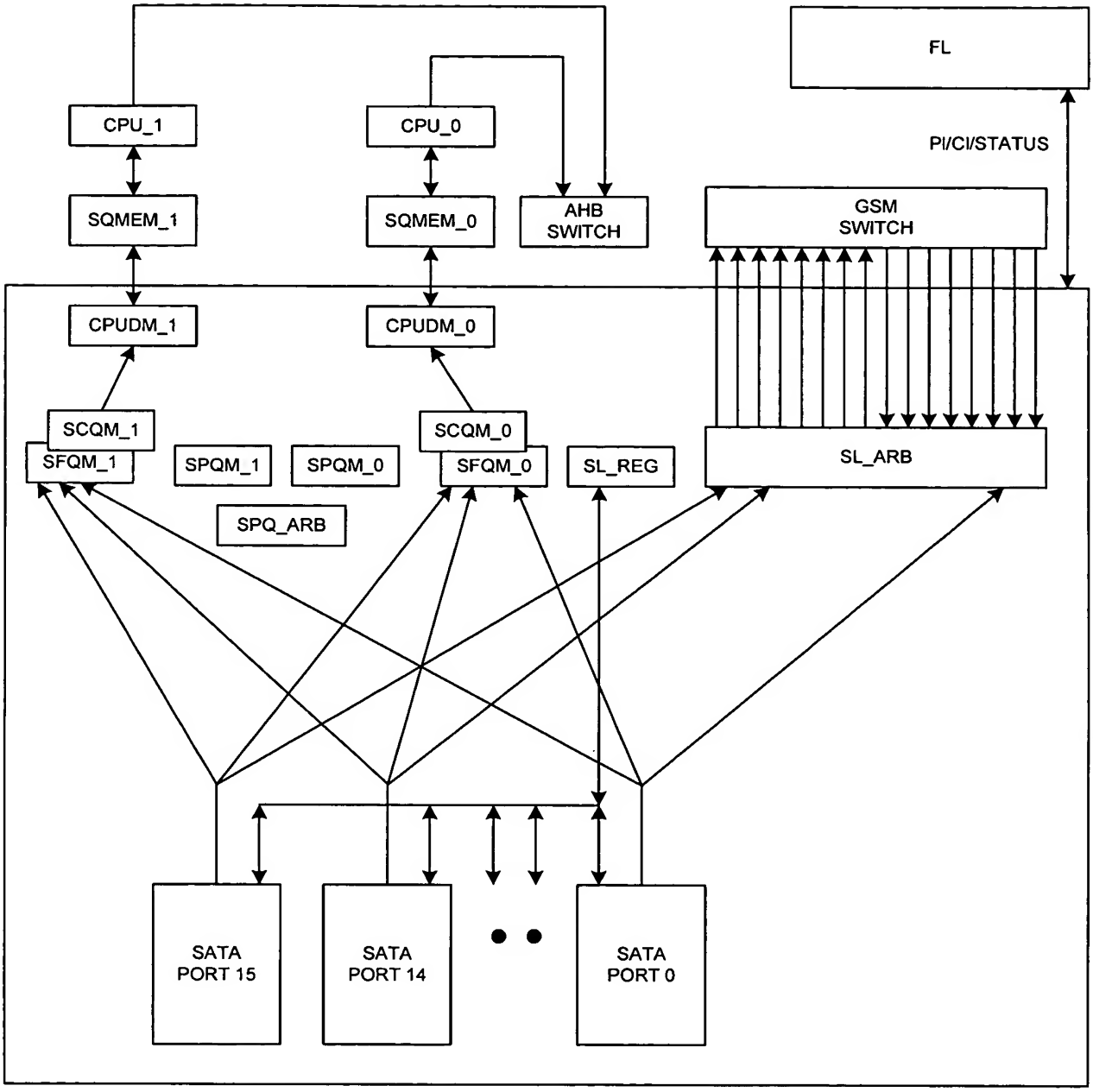

FL
PI/CI/STATUS
CPU_1
CPU_0
SQMEM_1
SQMEM_0
AHB SWITCH
GSM SWITCH
CPUDM_1
CPUDM_0
SCQM_1
SFQM_1
SPQM_1
SPQM_0
SCQM_0
SFQM_0
SL_REG
SL_ARB
SPQ_ARB
SATA PORT 15
SATA PORT 14
SATA PORT 0

Figure 22

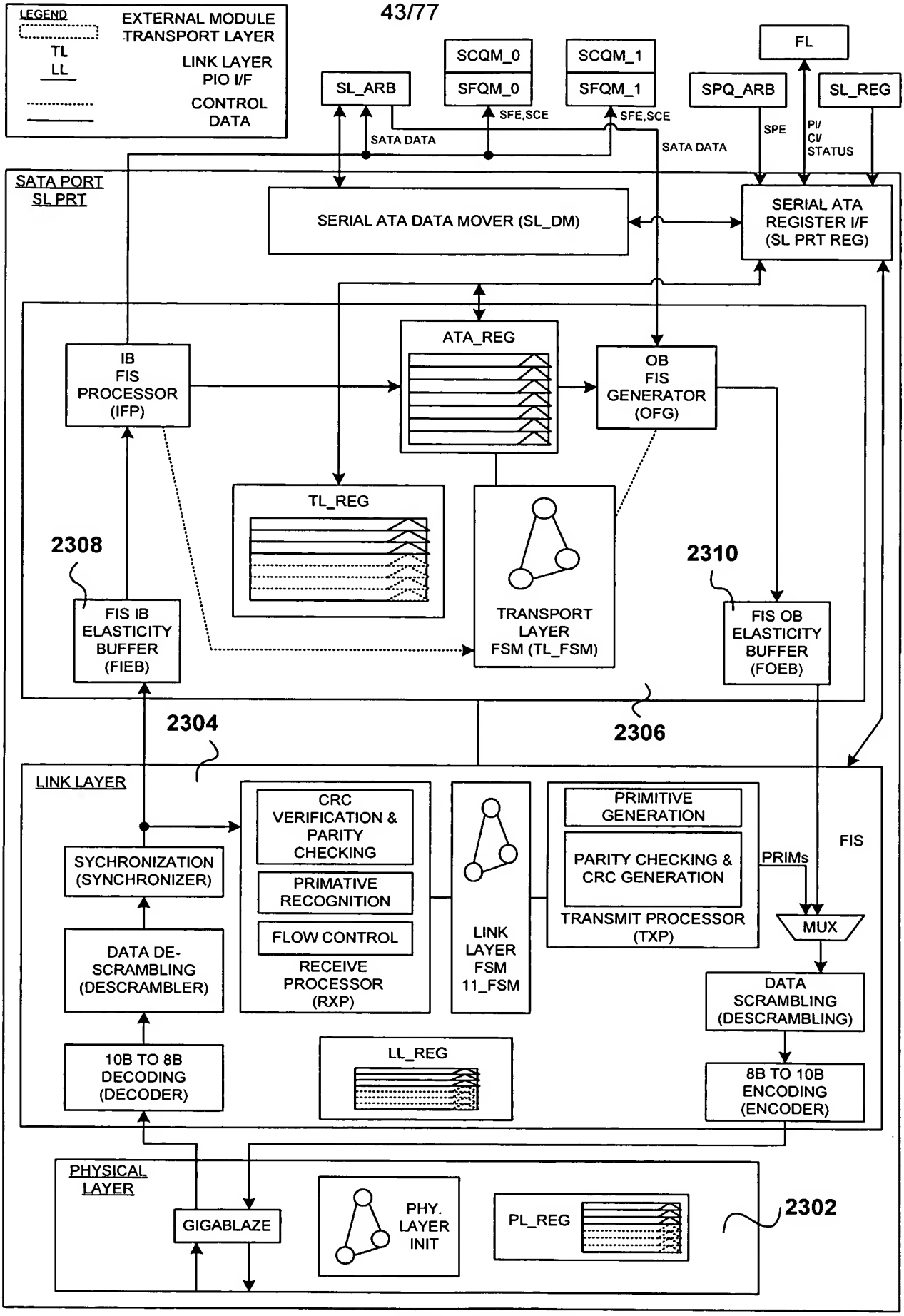

LEGEND
EXTERNAL MODULE
TRANSPORT LAYER
TL
LL
LINK LAYER
PIO I/F
CONTROL
DATA
SL_ARB
SCQM_0
SFQM_0
SCQM_1
SFQM_1
FL
SPQ_ARB
SL_REG
SFE,SCE
SFE,SCE
SATA DATA
SATA DATA
SPE
PI/
CI/
STATUS
SATA PORT
SL PRT
SERIAL ATA DATA MOVER (SL_DM)
SERIAL ATA
REGISTER I/F
(SL PRT REG)
ATA_REG
IB
FIS
PROCESSOR
(IFP)
OB
FIS
GENERATOR
(OFG)
TL_REG
2308
2310
FIS IB
ELASTICITY
BUFFER
(FIEB)
TRANSPORT
LAYER
FSM (TL_FSM)
FIS OB
ELASTICITY
BUFFER
(FOEB)
2304
2306
LINK LAYER
CRC
VERIFICATION &
PARITY
CHECKING
PRIMATIVE
RECOGNITION
FLOW CONTROL
RECEIVE
PROCESSOR
(RXP)
LINK
LAYER
FSM
11_FSM
PRIMITIVE
GENERATION
PARITY CHECKING &
CRC GENERATION
TRANSMIT PROCESSOR
(TXP)
PRIMs
FIS
MUX
SYCHRONIZATION
(SYNCHRONIZER)
DATA DE-
SCRAMBLING
(DESCRAMBLER)
DATA
SCRAMBLING
(DESCRAMBLING)
10B TO 8B
DECODING
(DECODER)
LL_REG
8B TO 10B
ENCODING
(ENCODER)
PHYSICAL
LAYER
GIGABLAZE
PHY.
LAYER
INIT
PL_REG
2302

Figure 23

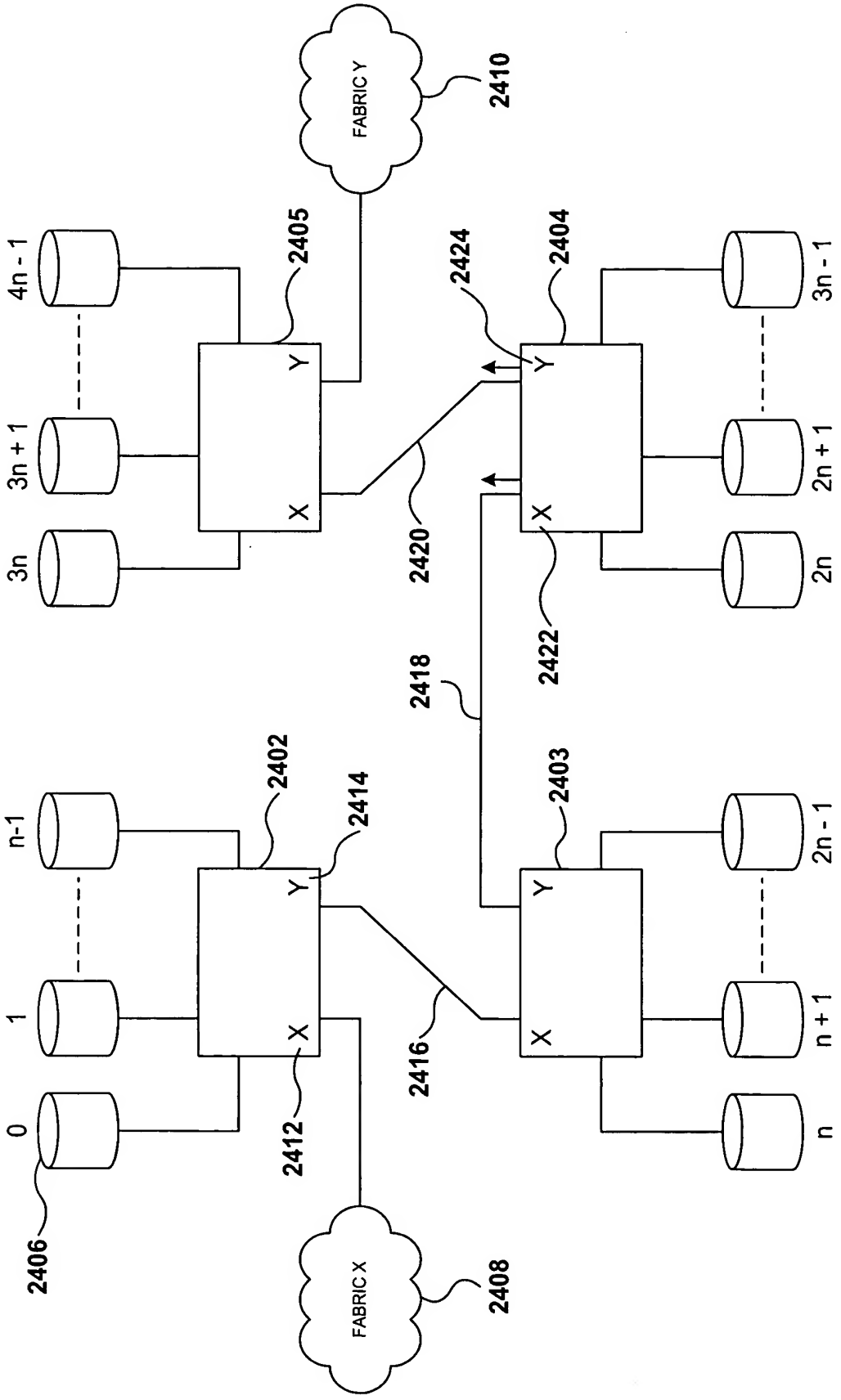

FABRIC Y
2410
FABRIC X
2408
2405
2404
2402
2403
2424
2414
2420
2418
2422
2416
2412
2406
4n - 1
3n + 1
3n
3n - 1
2n + 1
2n
n-1
1
0
2n - 1
n + 1
n
Y
X

Figure 24

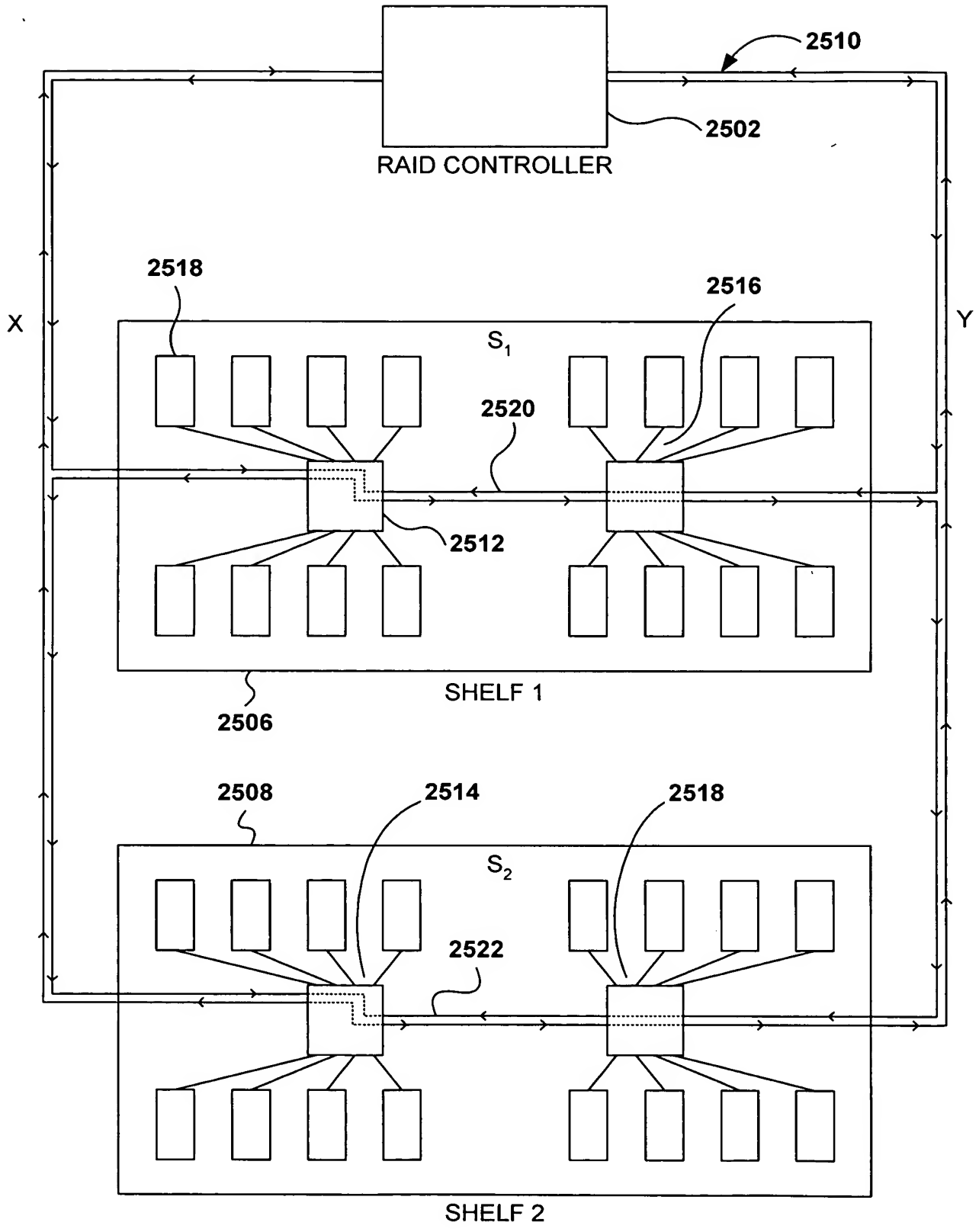

2510
2502
RAID CONTROLLER
2518
2516
X
Y
S1
2520
2512
SHELF 1
2506
2508
2514
2518
S2
2522
SHELF 2

Figure 25

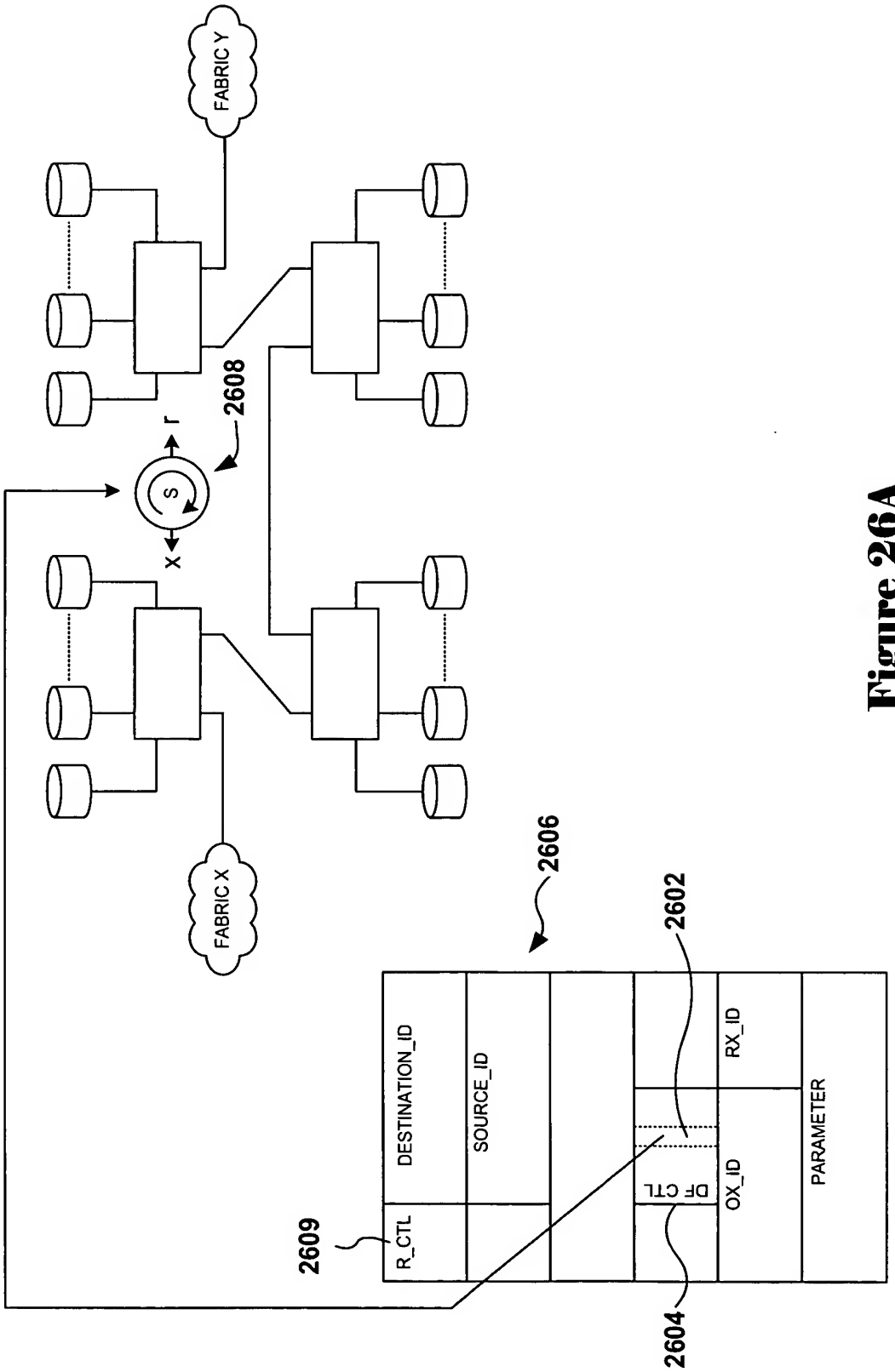

FABRIC Y
FABRIC X
2608
r
S
x
2606
2602
2609
2604
R_CTL
DESTINATION_ID
SOURCE_ID
DF CTL
OX_ID
RX_ID
PARAMETER

Figure 26A

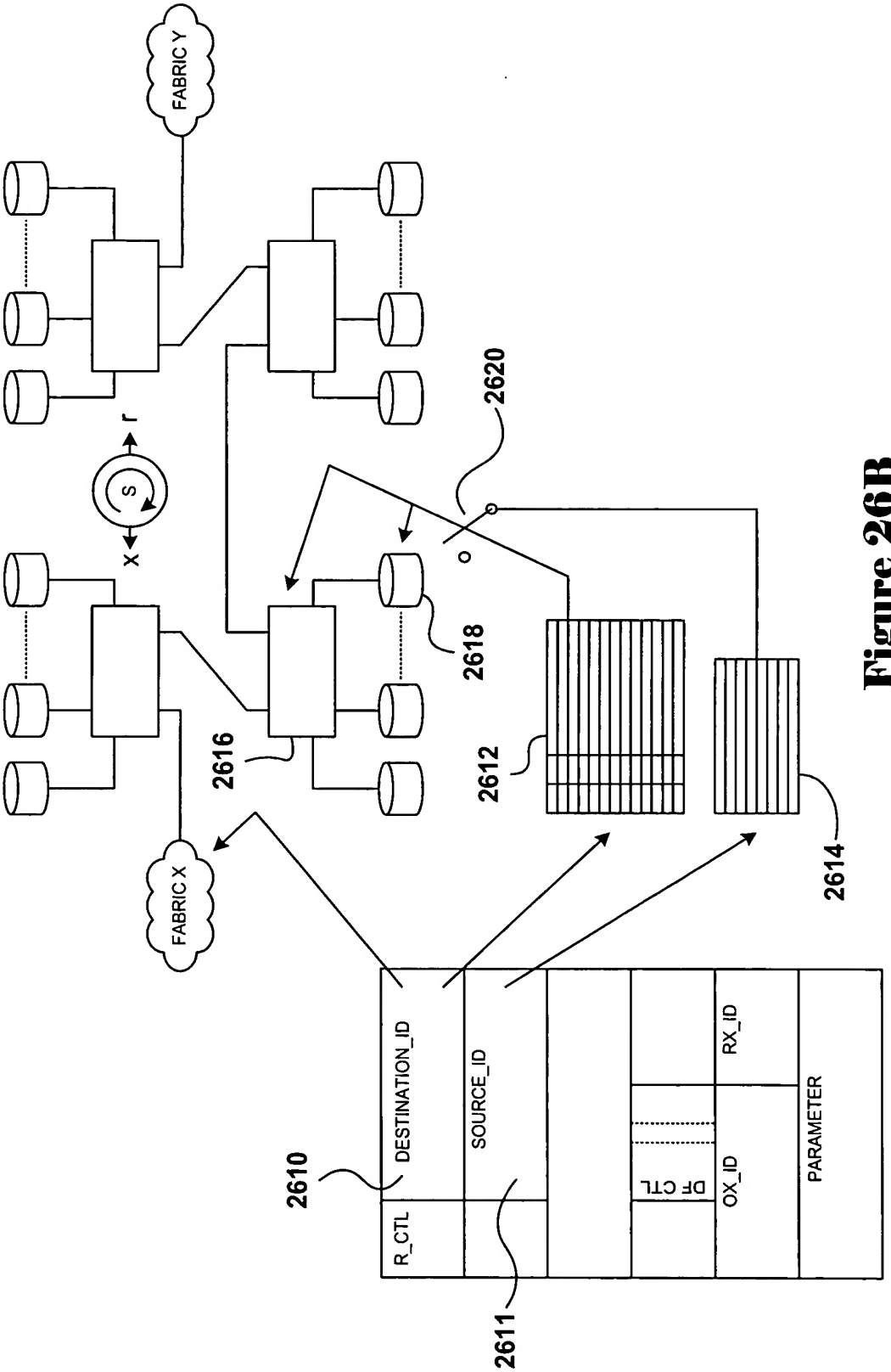

FABRIC Y
FABRIC X
r
s
x
o
2610
2611
2612
2614
2616
2618
2620
R_CTL
DESTINATION_ID
SOURCE_ID
DF CTL
OX_ID
RX_ID
PARAMETER

Figure 26B

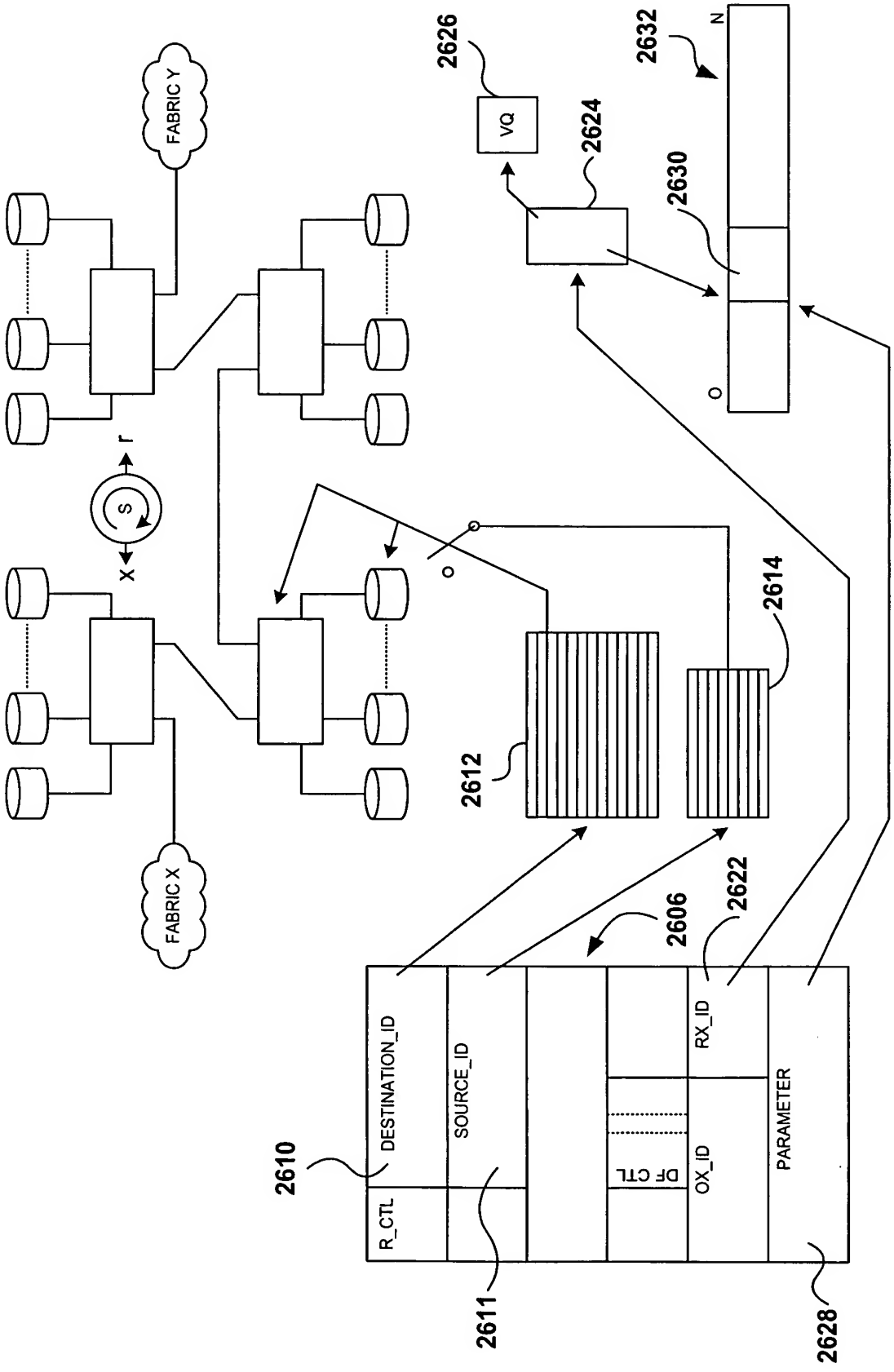

FABRIC Y
FABRIC X
S
r
x
o
2626
VQ
2624
2630
2632
N
0
2612
2614
2606
2622
2610
2611
2628
R_CTL
DESTINATION_ID
SOURCE_ID
DF CTL
OX_ID
RX_ID
PARAMETER

Figure 26C

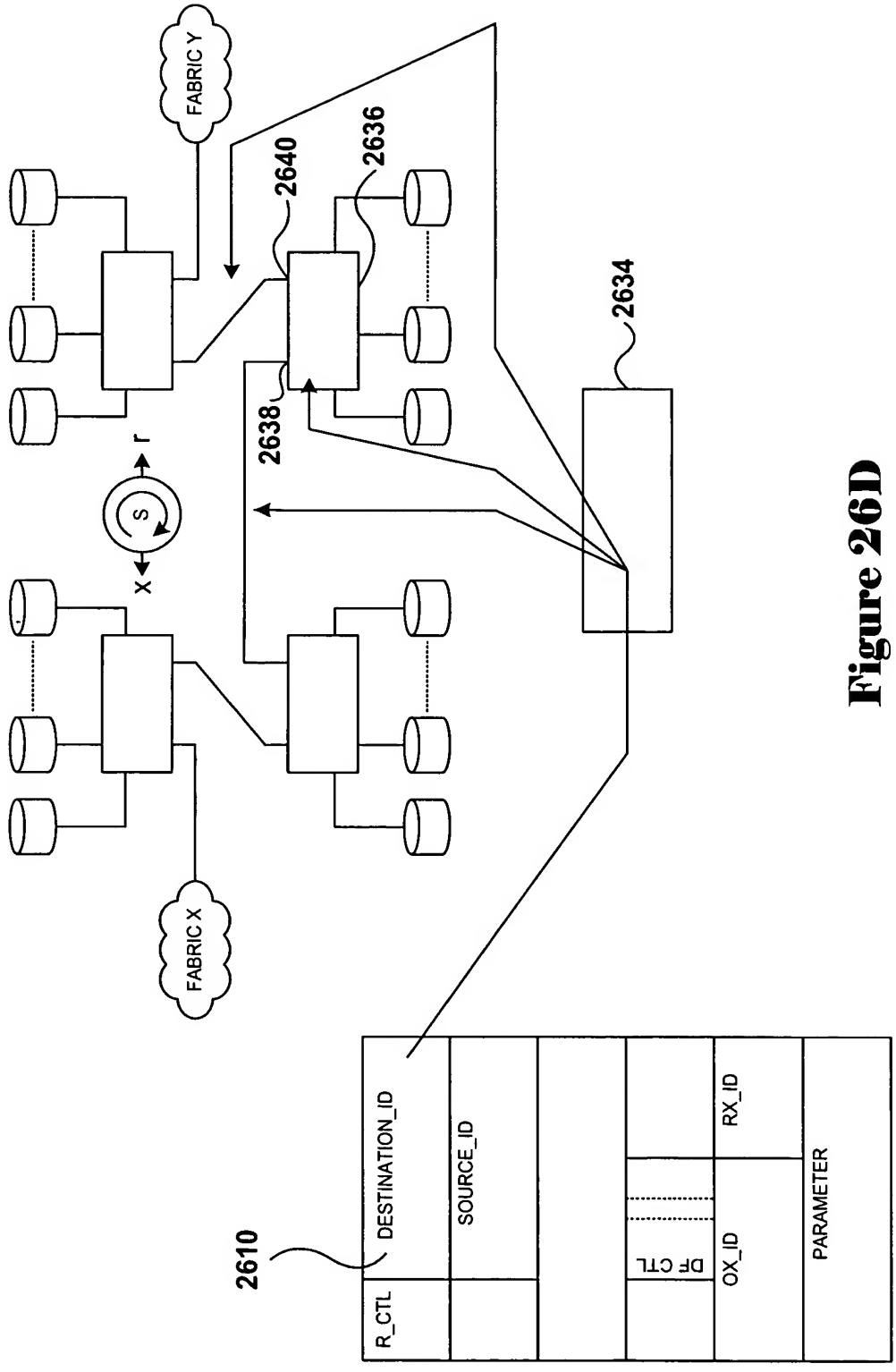
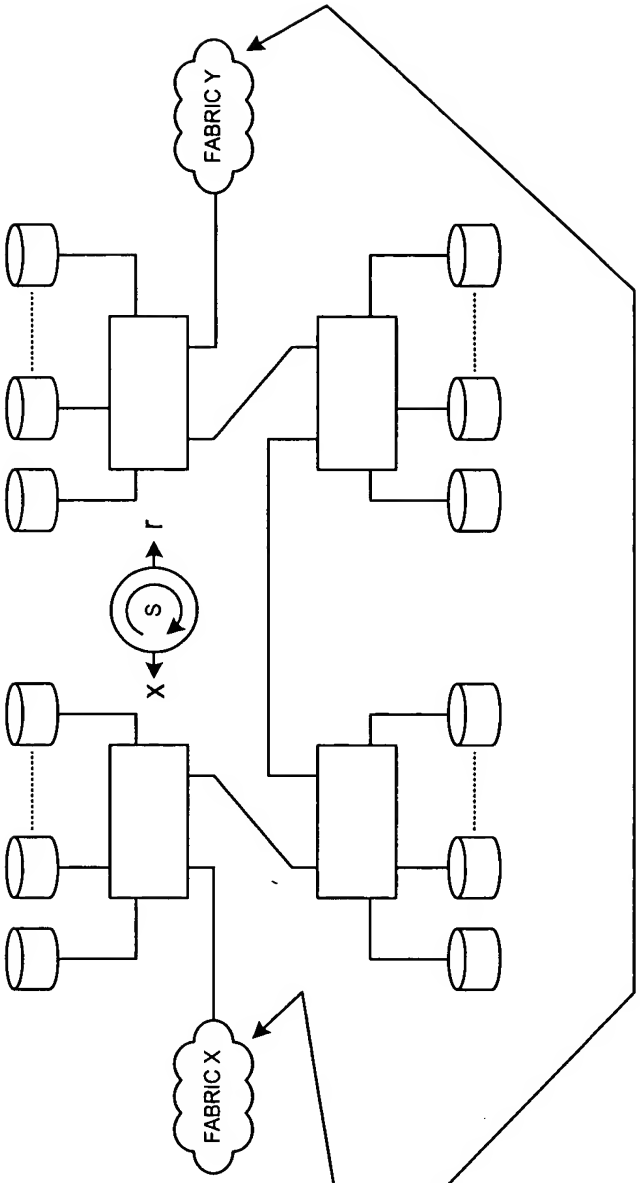
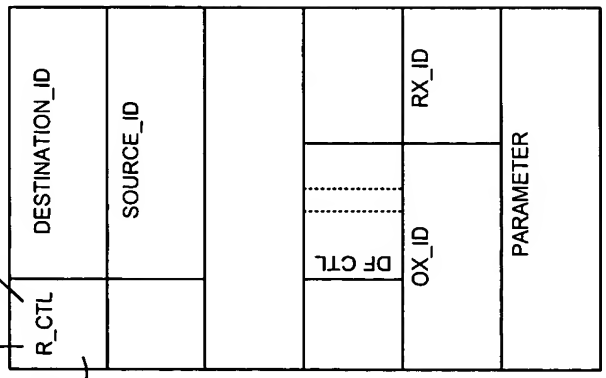

FABRIC Y
2640
2636
2634
2638
r
S
x
FABRIC X
2610
R_CTL
DESTINATION_ID
SOURCE_ID
DF CTL
OX_ID
RX_ID
PARAMETER

Figure 26D





2642

Figure 26E

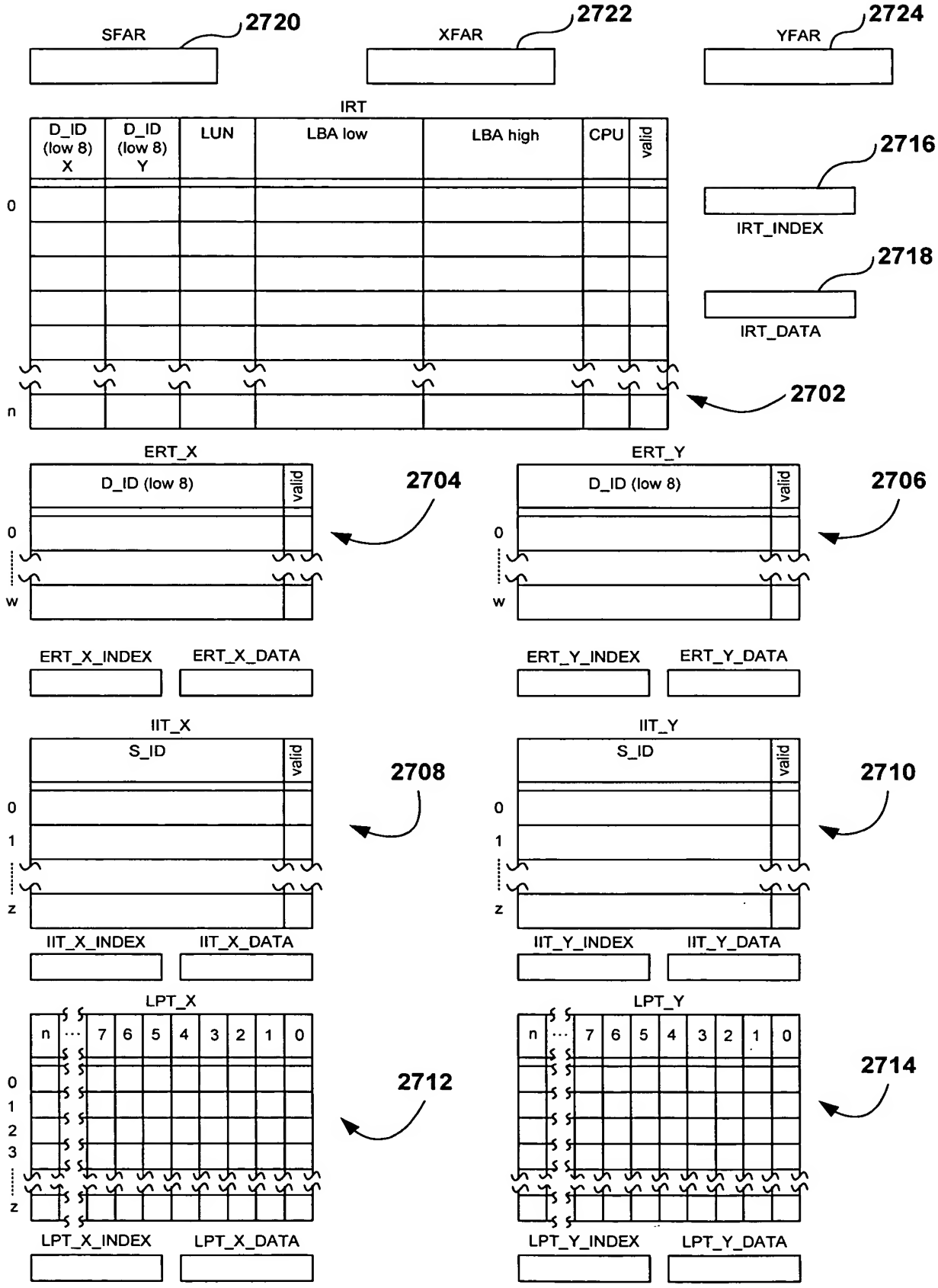

SFAR
2720
XFAR
2722
YFAR
2724
IRT
D_ID (low 8) X
D_ID (low 8) Y
LUN
LBA low
LBA high
CPU
valid
0
n
2716
IRT_INDEX
2718
IRT_DATA
2702
ERT_X
D_ID (low 8)
valid
2704
0
w
ERT_X_INDEX
ERT_X_DATA
ERT_Y
D_ID (low 8)
valid
2706
0
w
ERT_Y_INDEX
ERT_Y_DATA
IIT_X
S_ID
valid
2708
0
1
z
IIT_X_INDEX
IIT_X_DATA
IIT_Y
S_ID
valid
2710
0
1
z
IIT_Y_INDEX
IIT_Y_DATA
LPT_X
n
7
6
5
4
3
2
1
0
2712
0
1
2
3
z
LPT_X_INDEX
LPT_X_DATA
LPT_Y
n
7
6
5
4
3
2
1
0
2714
LPT_Y_INDEX
LPT_Y_DATA

Figure 27

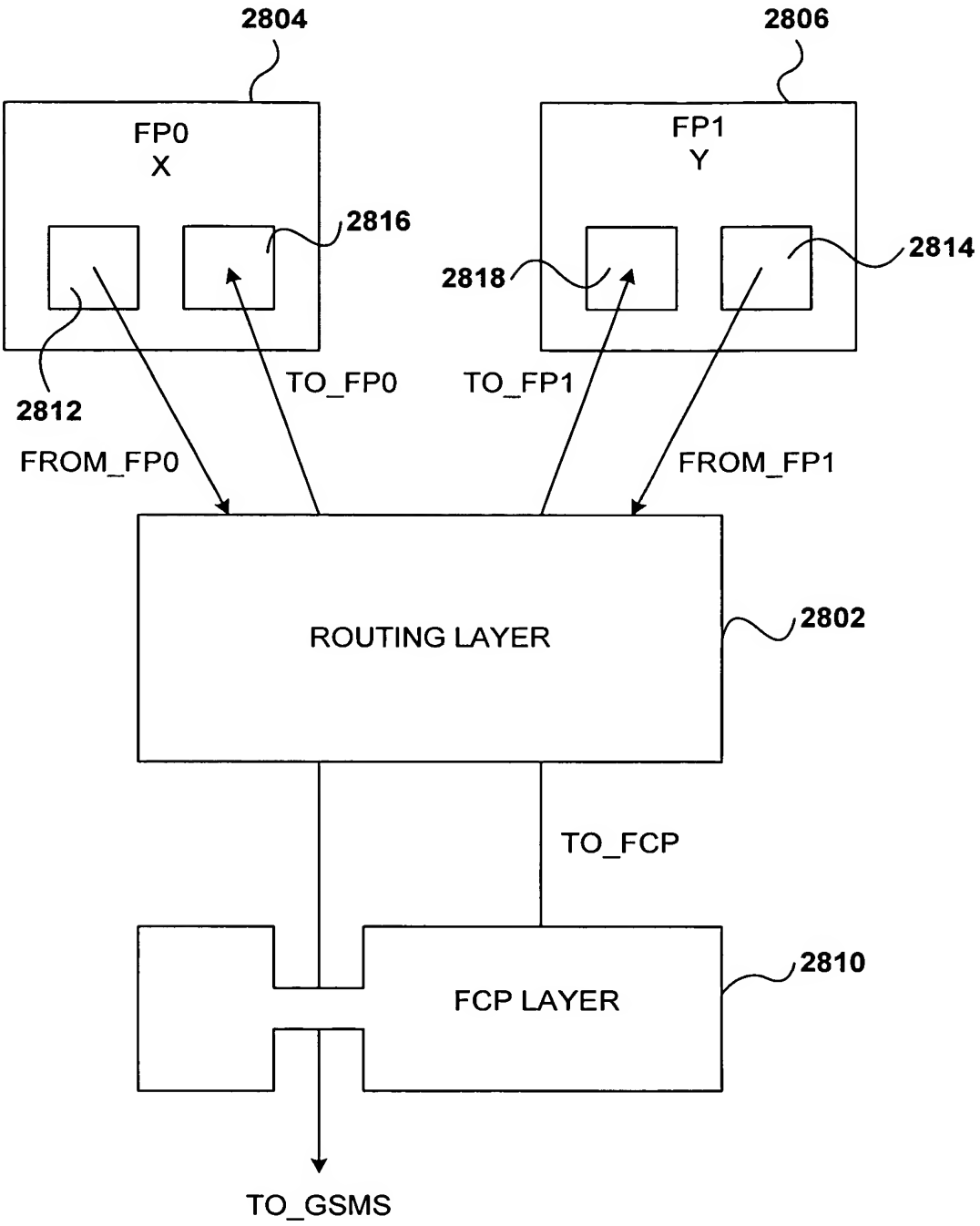

2804
2806
FP0
X
FP1
Y
2816
2814
2818
2812
TO_FP0
TO_FP1
FROM_FP0
FROM_FP1
ROUTING LAYER
2802
TO_FCP
FCP LAYER
2810
TO_GSMS

Figure 28

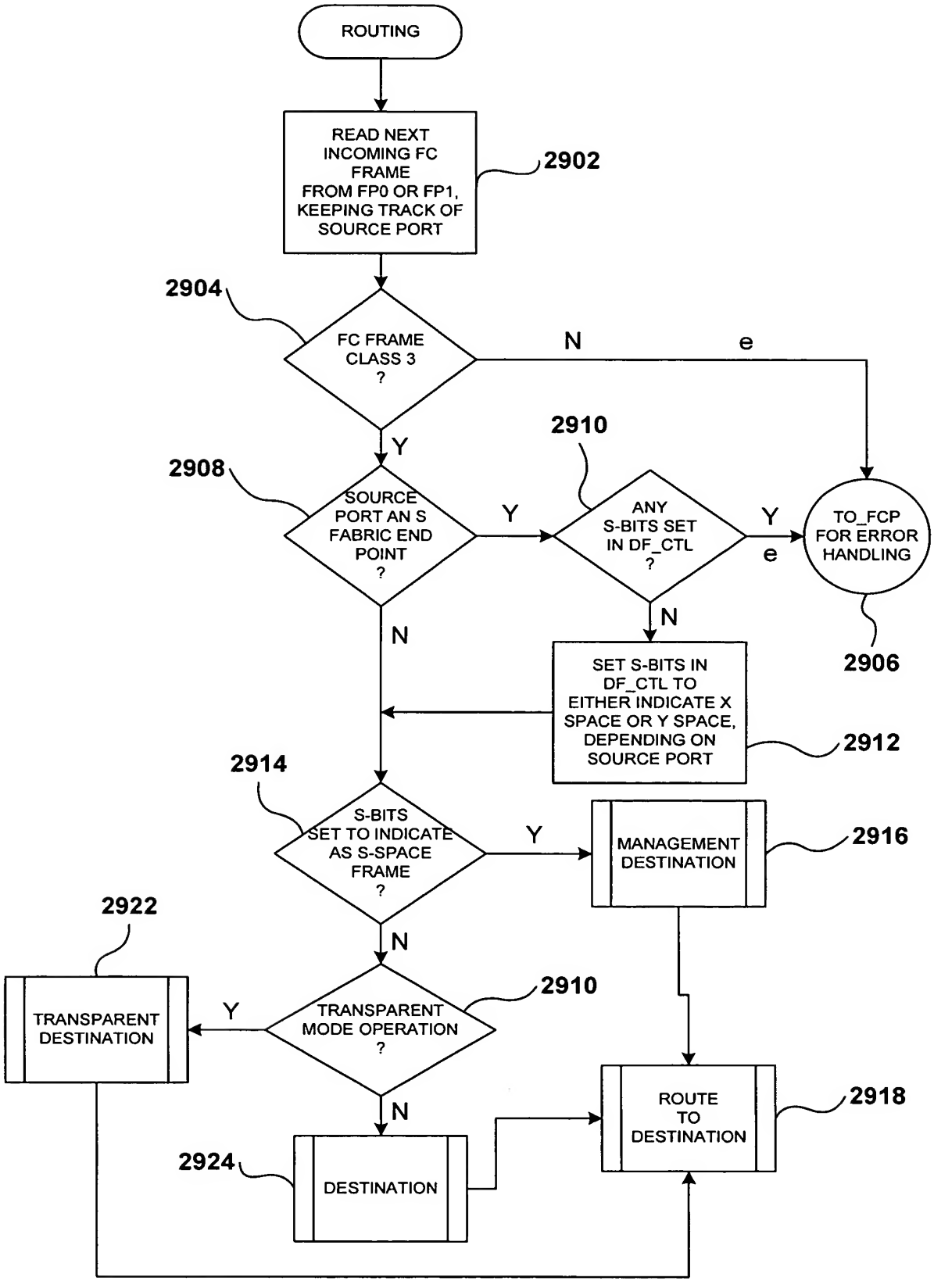

ROUTING
READ NEXT INCOMING FC FRAME FROM FP0 OR FP1, KEEPING TRACK OF SOURCE PORT
2902
2904
FC FRAME CLASS 3 ?
N
e
Y
2910
2908
SOURCE PORT AN S FABRIC END POINT ?
Y
ANY S-BITS SET IN DF_CTL ?
Y
e
TO_FCP FOR ERROR HANDLING
2906
N
N
SET S-BITS IN DF_CTL TO EITHER INDICATE X SPACE OR Y SPACE, DEPENDING ON SOURCE PORT
2912
2914
S-BITS SET TO INDICATE AS S-SPACE FRAME ?
Y
MANAGEMENT DESTINATION
2916
2922
N
TRANSPARENT DESTINATION
Y
TRANSPARENT MODE OPERATION ?
2910
N
ROUTE TO DESTINATION
2918
2924
DESTINATION

Figure 29

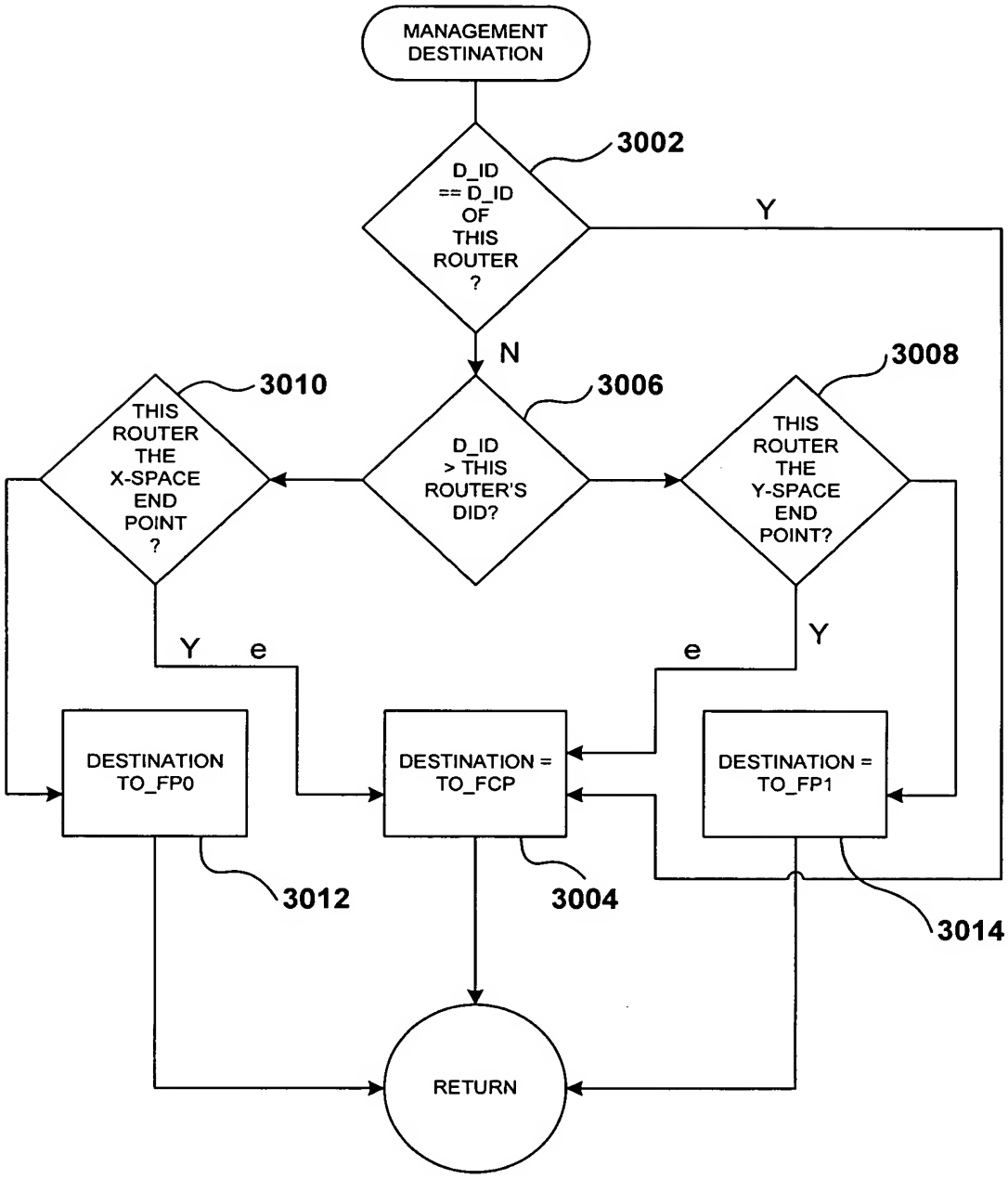

MANAGEMENT DESTINATION
D_ID == D_ID OF THIS ROUTER ?
3002
Y
N
THIS ROUTER THE X-SPACE END POINT ?
3010
D_ID > THIS ROUTER'S DID?
3006
THIS ROUTER THE Y-SPACE END POINT?
3008
Y
e
e
Y
DESTINATION TO_FP0
DESTINATION = TO_FCP
DESTINATION = TO_FP1
3012
3004
3014
RETURN

Figure 30

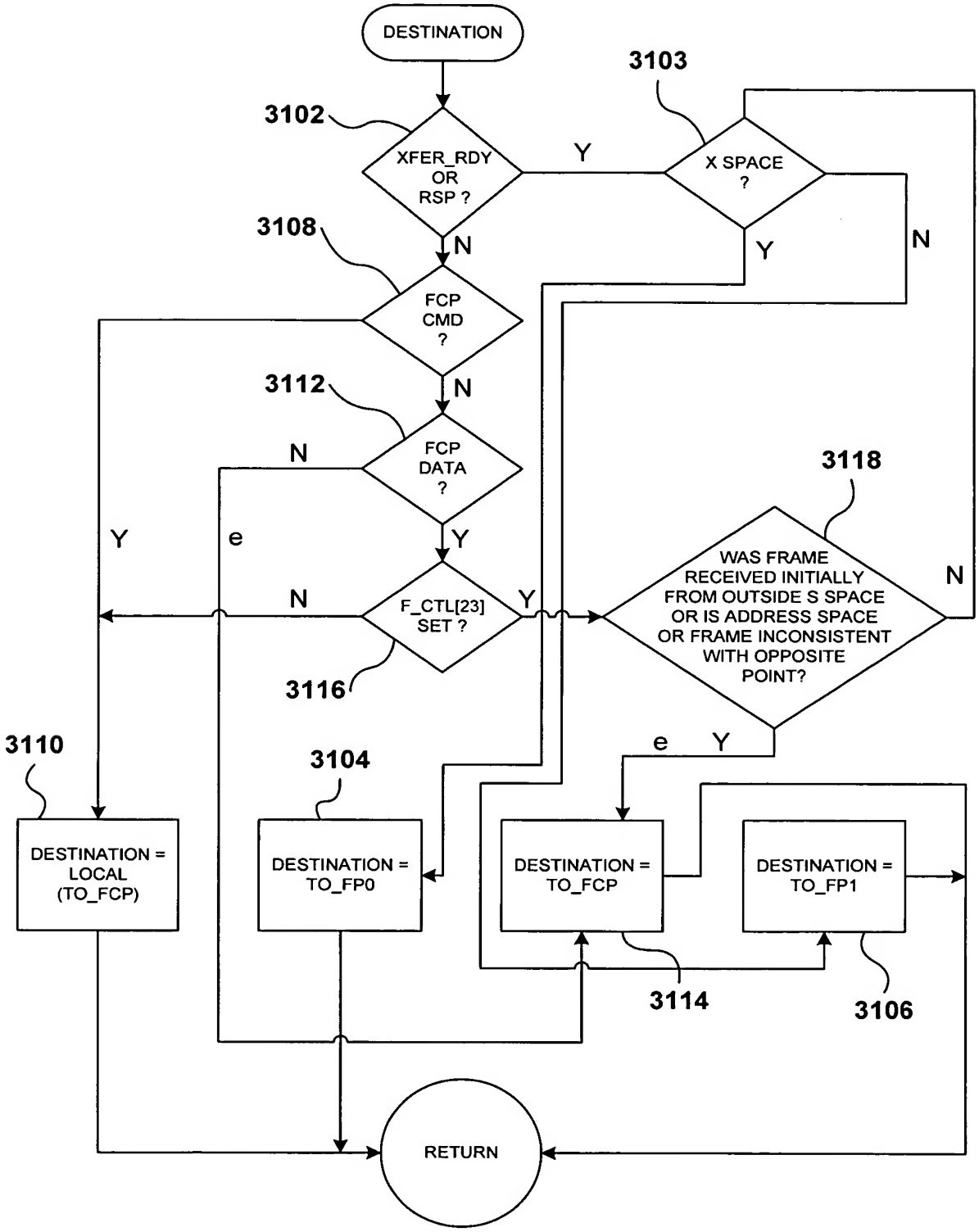

DESTINATION
3103
3102
XFER_RDY OR RSP ?
Y
X SPACE ?
N
Y
N
3108
FCP CMD ?
N
3112
FCP DATA ?
N
Y
e
Y
N
3118
F_CTL[23] SET ?
N
Y
WAS FRAME RECEIVED INITIALLY FROM OUTSIDE S SPACE OR IS ADDRESS SPACE OR FRAME INCONSISTENT WITH OPPOSITE POINT?
N
3116
e
Y
3110
3104
DESTINATION = LOCAL (TO_FCP)
DESTINATION = TO_FP0
DESTINATION = TO_FCP
DESTINATION = TO_FP1
3114
3106
RETURN

Figure 31

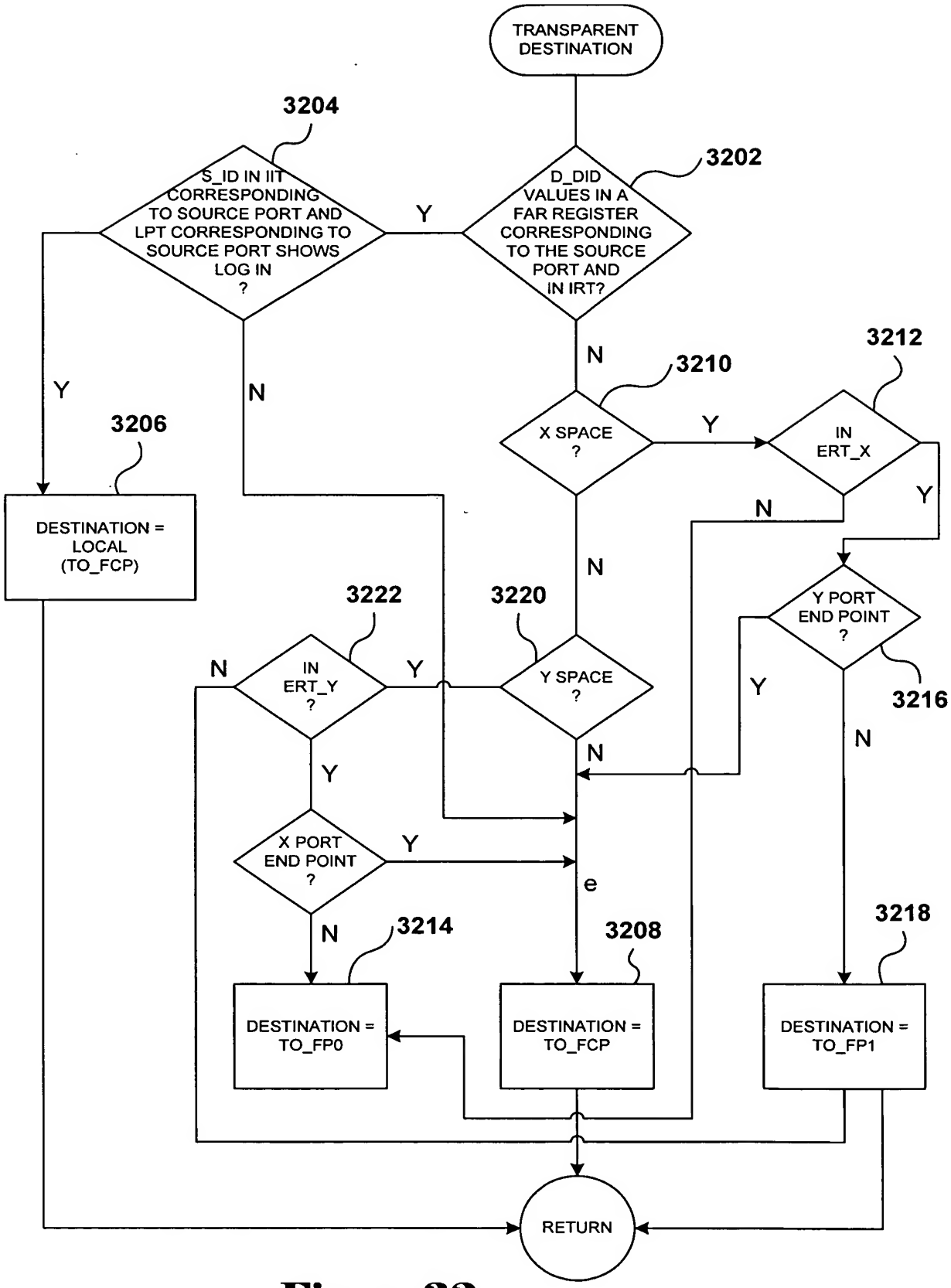

TRANSPARENT DESTINATION
3204
S_ID IN IIT CORRESPONDING TO SOURCE PORT AND LPT CORRESPONDING TO SOURCE PORT SHOWS LOG IN ?
Y
3202
D_DID VALUES IN A FAR REGISTER CORRESPONDING TO THE SOURCE PORT AND IN IRT?
Y
N
3212
3210
X SPACE ?
Y
IN ERT_X
Y
N
3206
DESTINATION = LOCAL (TO_FCP)
N
N
3222
3220
Y PORT END POINT ?
N
IN ERT_Y ?
Y
Y SPACE ?
Y
3216
N
N
Y
X PORT END POINT ?
Y
e
N
3214
3208
3218
DESTINATION = TO_FP0
DESTINATION = TO_FCP
DESTINATION = TO_FP1
RETURN

Figure 32

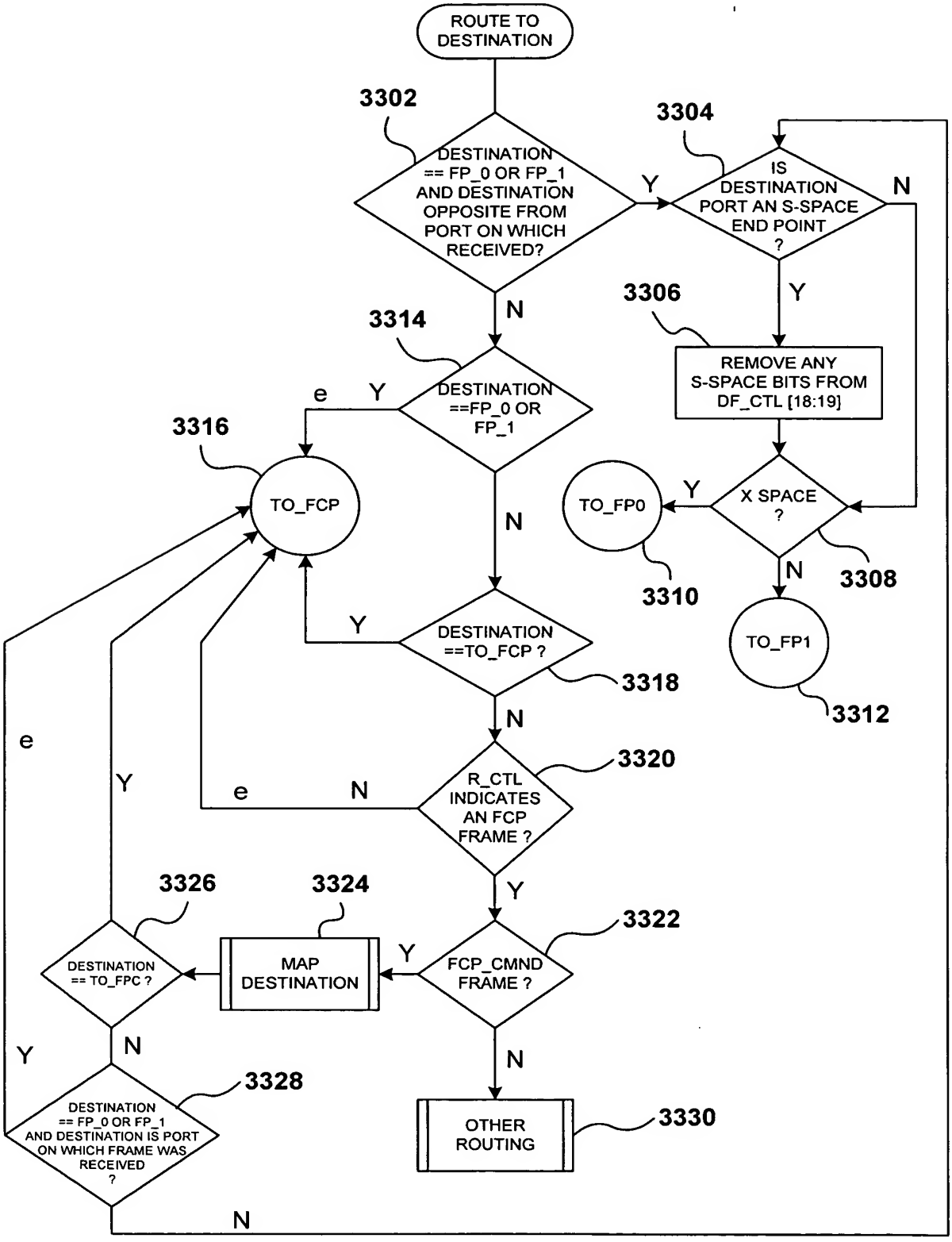

ROUTE TO DESTINATION
3302
DESTINATION == FP_0 OR FP_1 AND DESTINATION OPPOSITE FROM PORT ON WHICH RECEIVED?
Y
3304
IS DESTINATION PORT AN S-SPACE END POINT ?
N
Y
3306
REMOVE ANY S-SPACE BITS FROM DF_CTL [18:19]
N
3314
DESTINATION ==FP_0 OR FP_1
e
Y
3316
TO_FCP
N
X SPACE ?
Y
TO_FP0
3310
N
3308
TO_FP1
3312
DESTINATION ==TO_FCP ?
Y
3318
N
3320
R_CTL INDICATES AN FCP FRAME ?
e
N
Y
Y
3322
FCP_CMND FRAME ?
Y
3324
MAP DESTINATION
3326
DESTINATION == TO_FPC ?
N
Y
3328
DESTINATION == FP_0 OR FP_1 AND DESTINATION IS PORT ON WHICH FRAME WAS RECEIVED ?
N
OTHER ROUTING
3330
N
e
Y

Figure 33

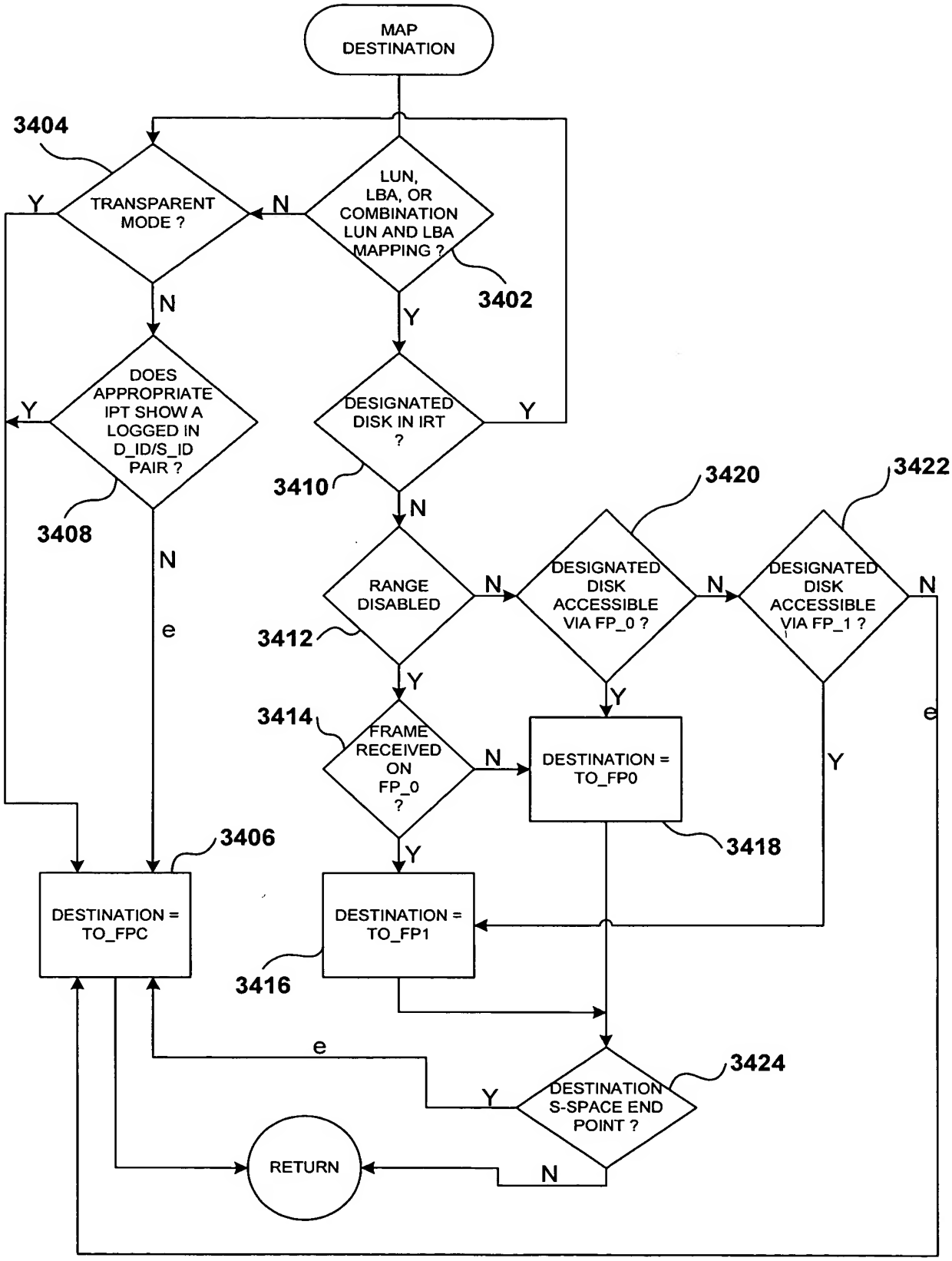

MAP DESTINATION
3404
TRANSPARENT MODE ?
Y
N
LUN, LBA, OR COMBINATION LUN AND LBA MAPPING ?
3402
N
Y
DOES APPROPRIATE IPT SHOW A LOGGED IN D_ID/S_ID PAIR ?
Y
3408
N
e
DESIGNATED DISK IN IRT ?
Y
3410
N
RANGE DISABLED
N
3412
Y
3420
DESIGNATED DISK ACCESSIBLE VIA FP_0 ?
N
Y
3422
DESIGNATED DISK ACCESSIBLE VIA FP_1 ?
N
e
Y
3414
FRAME RECEIVED ON FP_0 ?
N
Y
DESTINATION = TO_FP0
3418
3406
DESTINATION = TO_FPC
DESTINATION = TO_FP1
3416
e
Y
3424
DESTINATION S-SPACE END POINT ?
N
RETURN

Figure 34

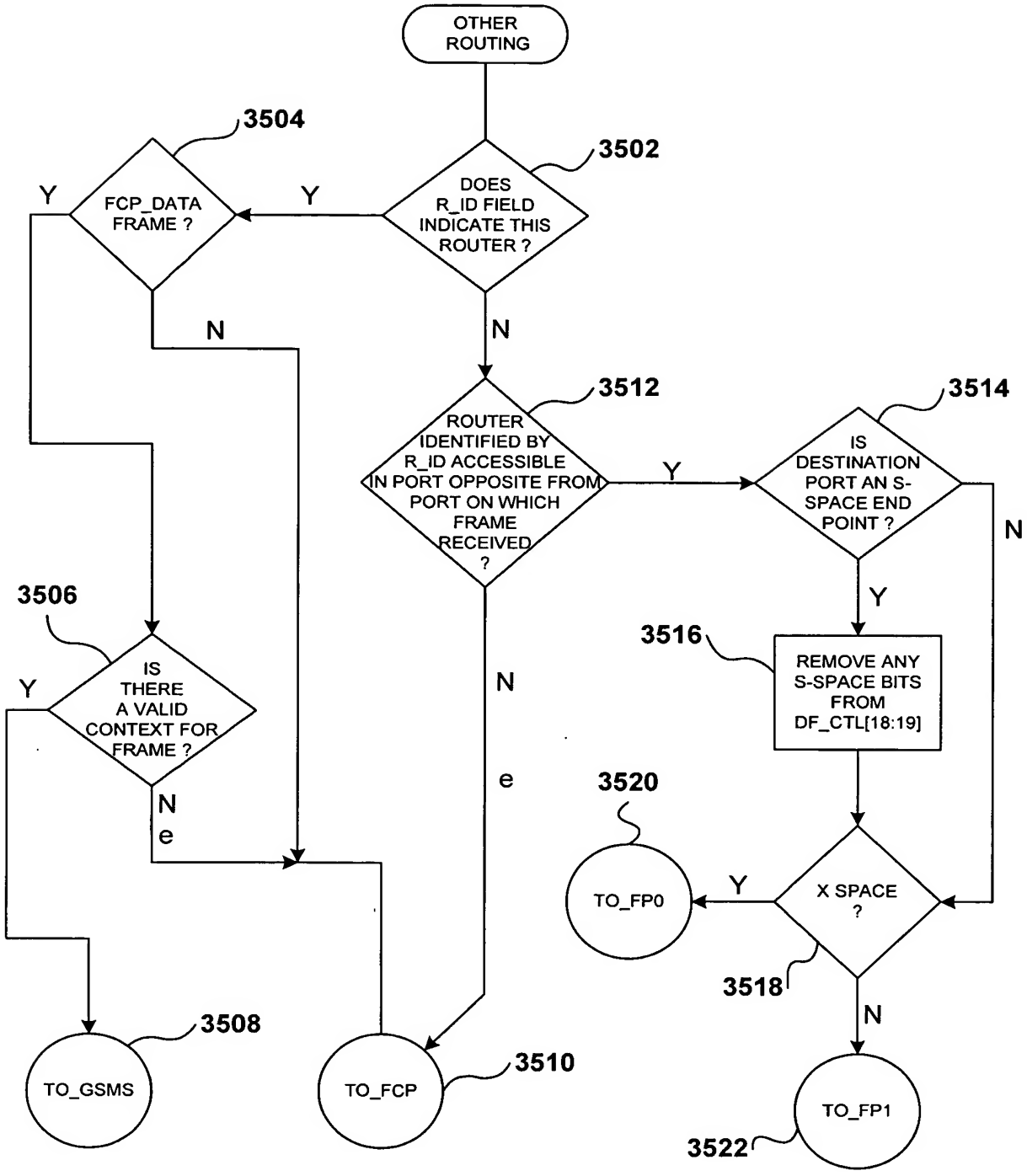

OTHER ROUTING
3502
DOES R_ID FIELD INDICATE THIS ROUTER ?
Y
3504
FCP_DATA FRAME ?
Y
N
N
3512
ROUTER IDENTIFIED BY R_ID ACCESSIBLE IN PORT OPPOSITE FROM PORT ON WHICH FRAME RECEIVED ?
Y
3514
IS DESTINATION PORT AN S-SPACE END POINT ?
N
Y
3516
REMOVE ANY S-SPACE BITS FROM DF_CTL[18:19]
3506
IS THERE A VALID CONTEXT FOR FRAME ?
Y
N
e
N
e
3520
TO_FP0
Y
X SPACE ?
3518
N
3508
TO_GSMS
TO_FCP
3510
TO_FP1
3522

Figure 35

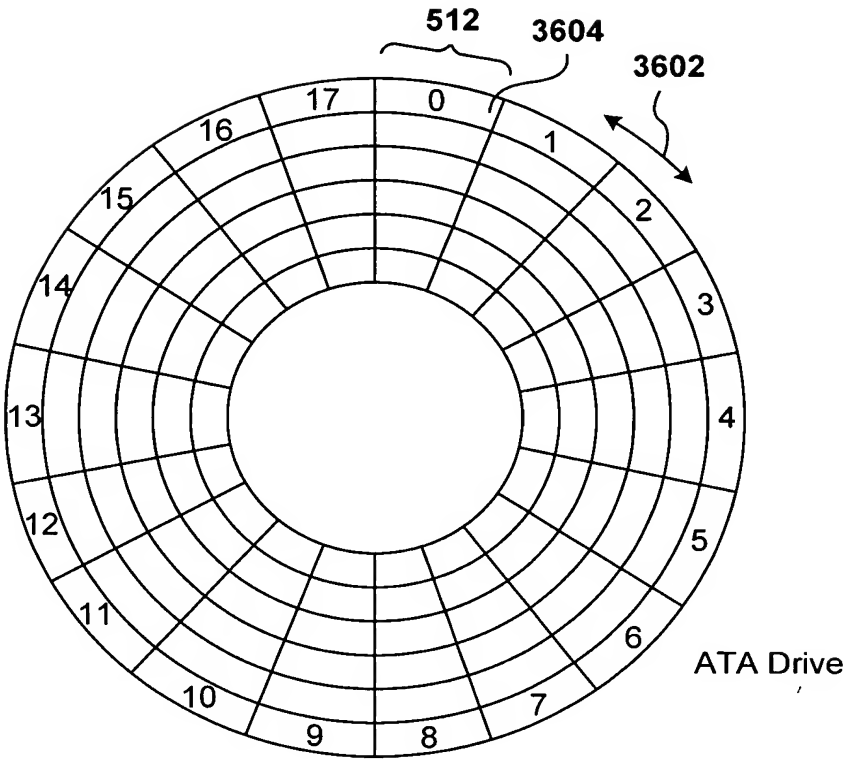


Figure 36A

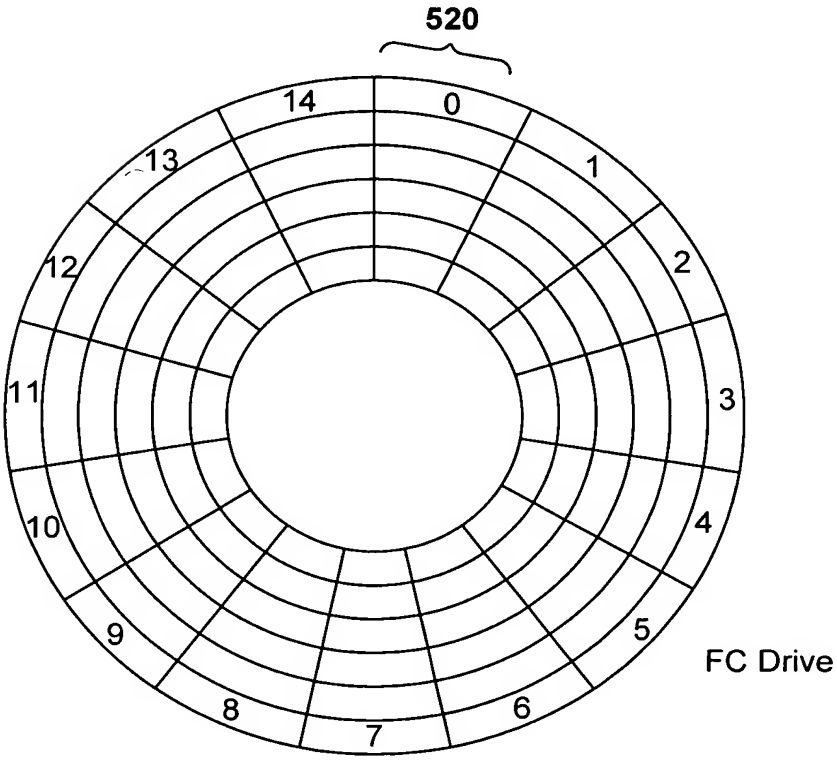


Figure 36B

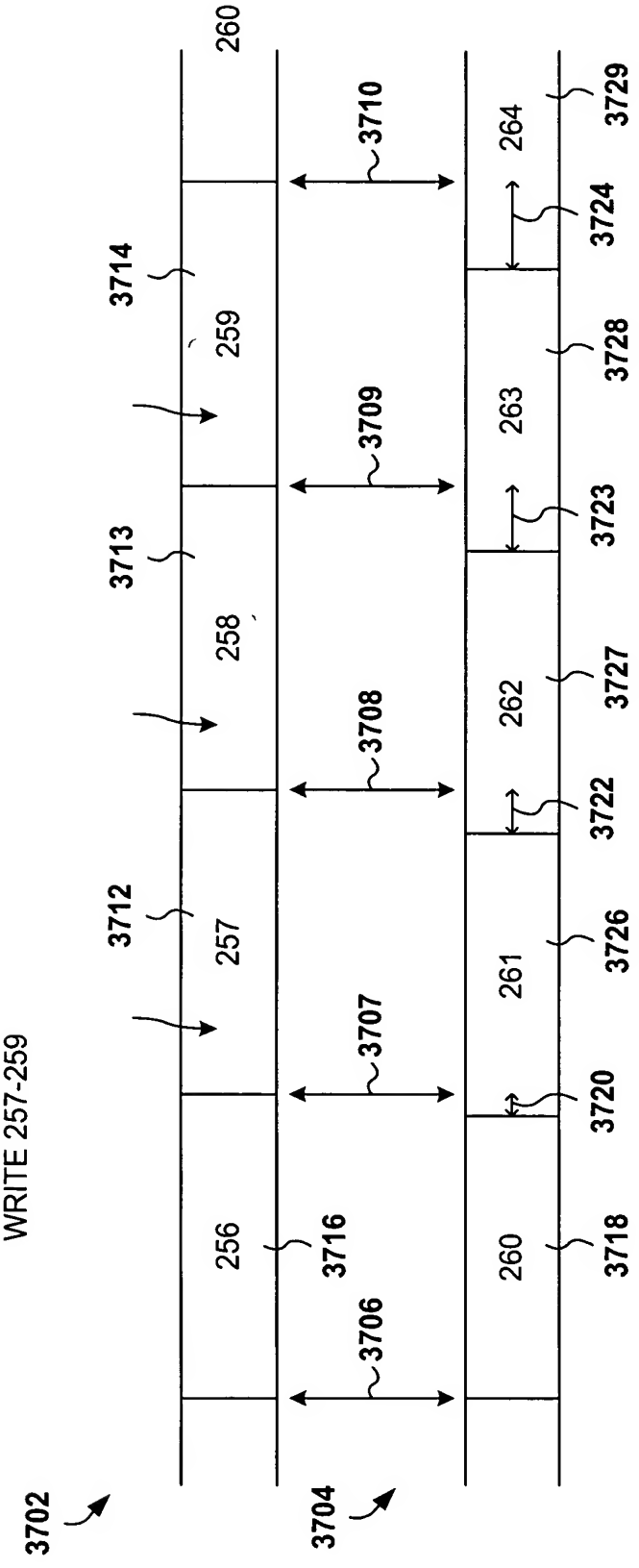

WRITE 257-259
3702
3704
3706
3707
3708
3709
3710
3712
3713
3714
3716
3718
3720
3722
3723
3724
3726
3727
3728
3729
256
257
258
259
260
260
261
262
263
264

Figure 37A

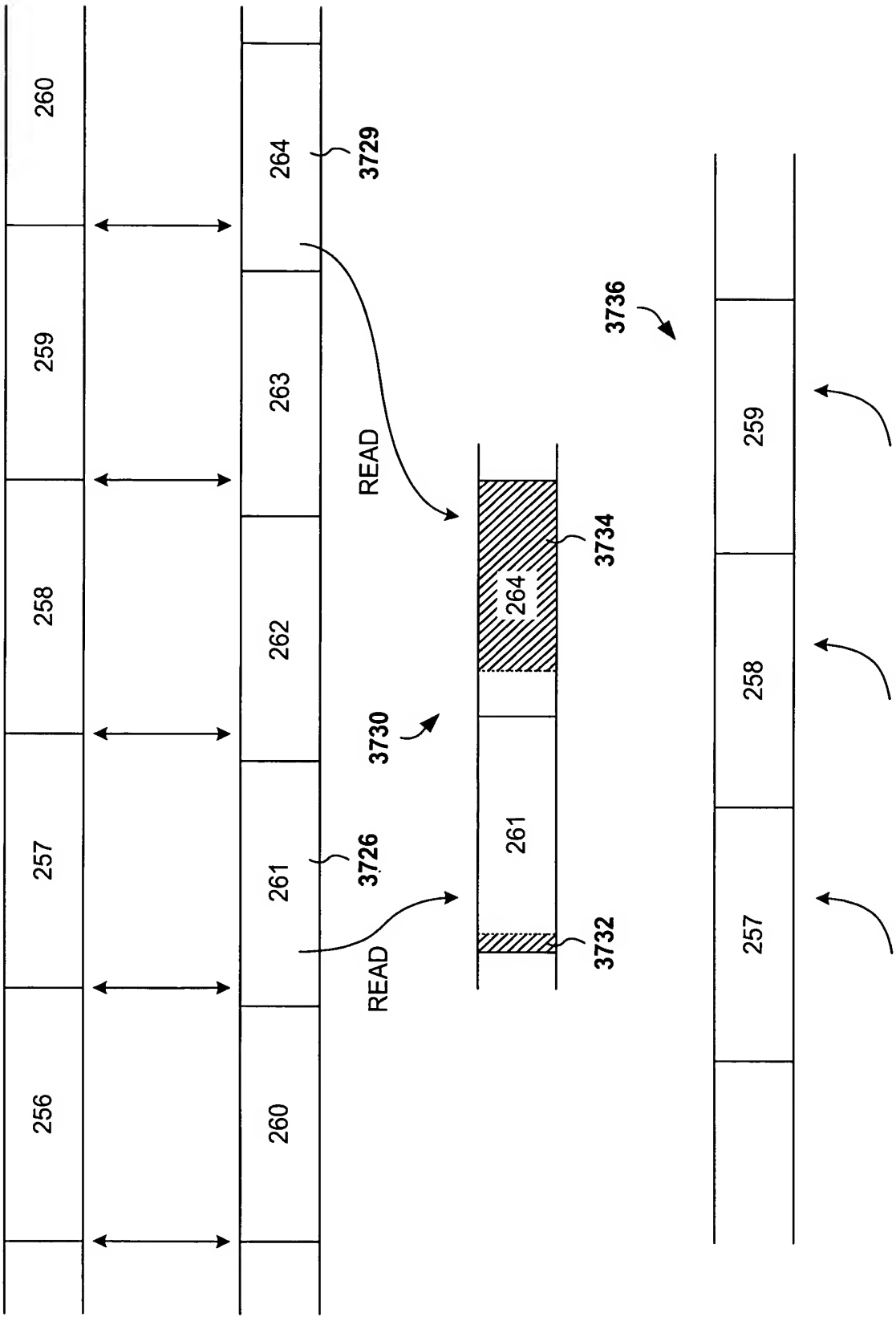

256
257
258
259
260
260
261
262
263
264
READ
READ
3726
3729
3730
3732
3734
3736
261
264
257
258
259

Figure 37B

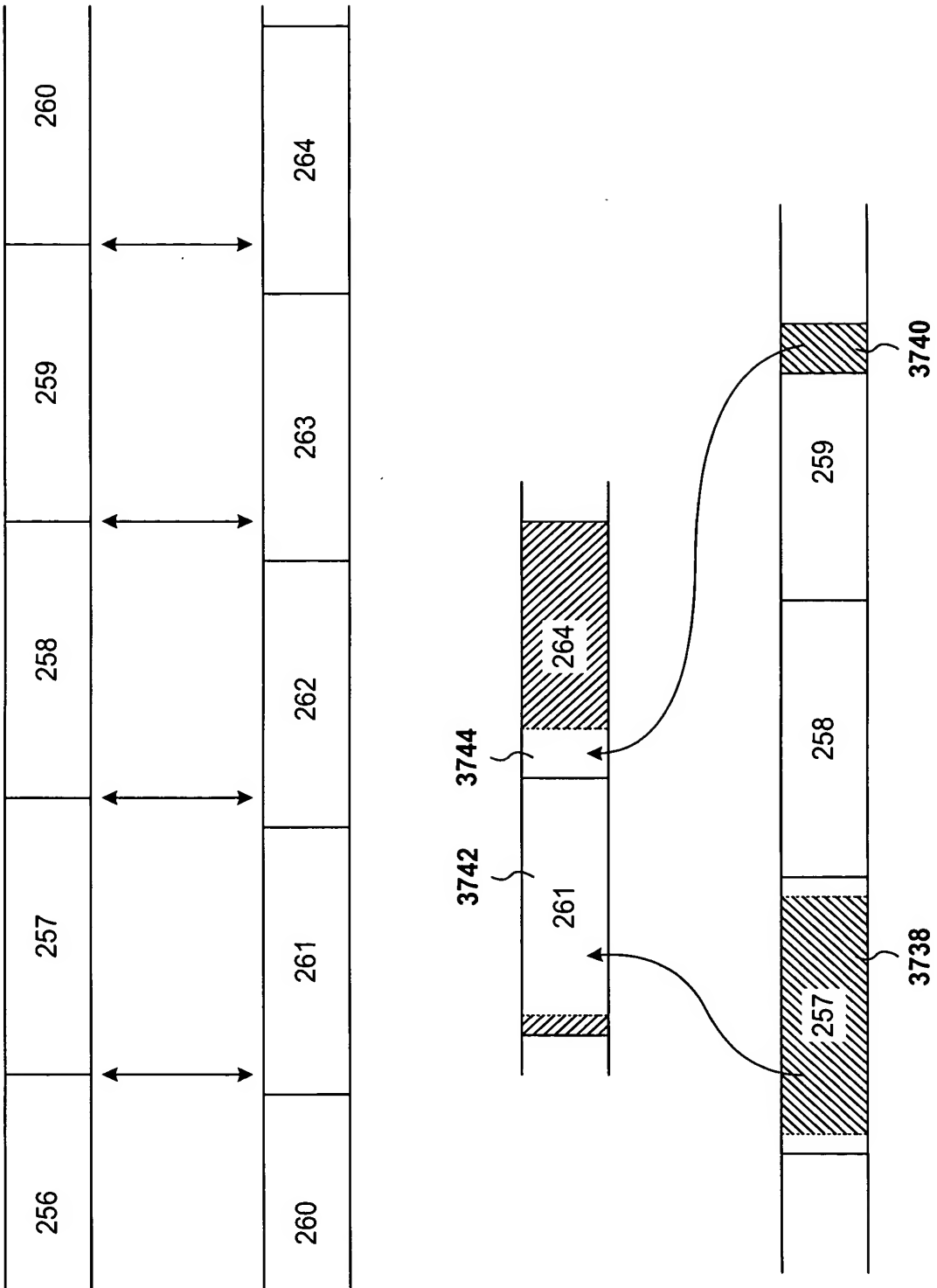

256
257
258
259
260
260
261
262
263
264
3744
3742
264
261
3740
259
258
257
3738

Figure 37C

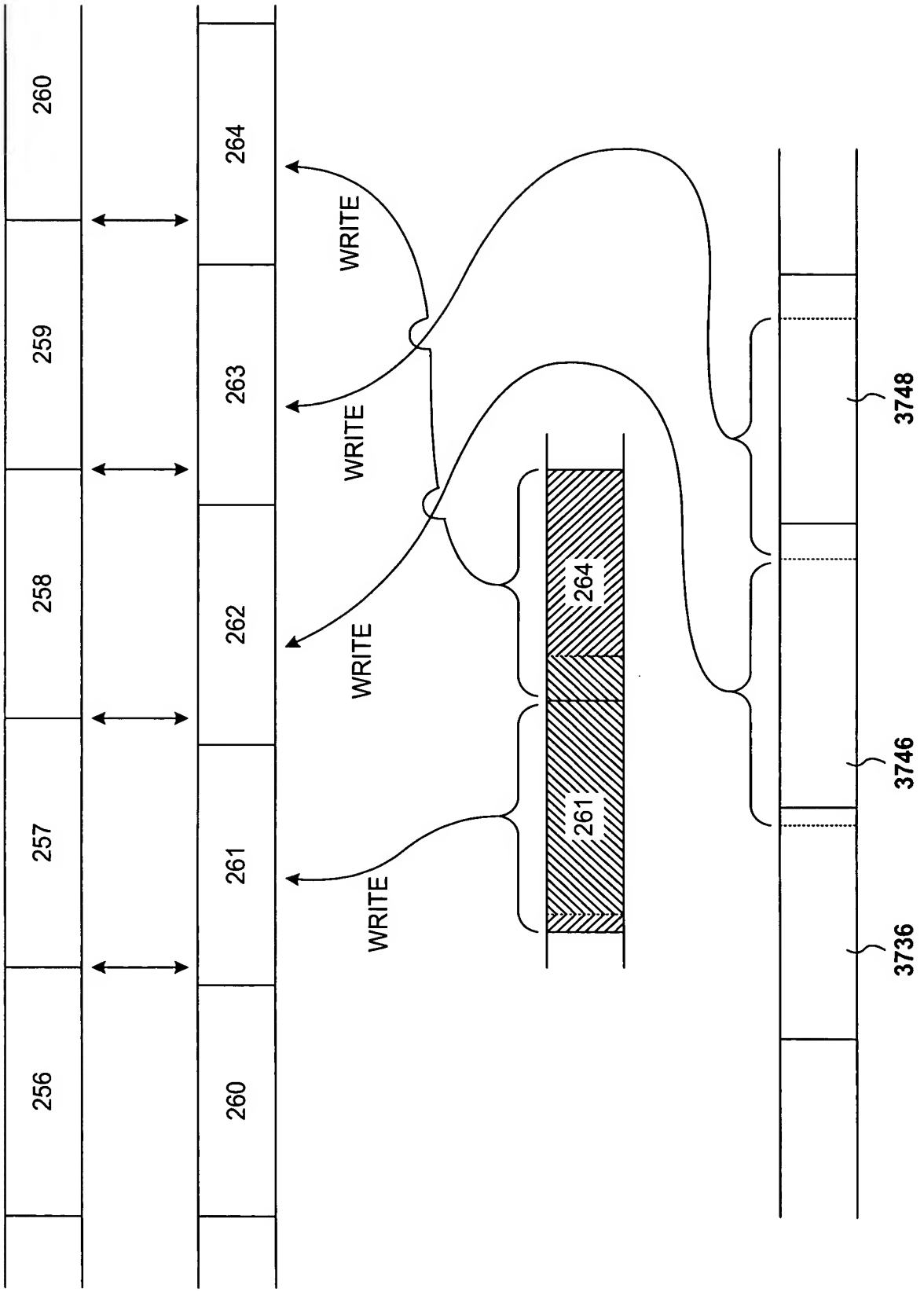

256
257
258
259
260
260
261
262
263
264
WRITE
WRITE
WRITE
WRITE
261
264
3736
3746
3748

Figure 37D

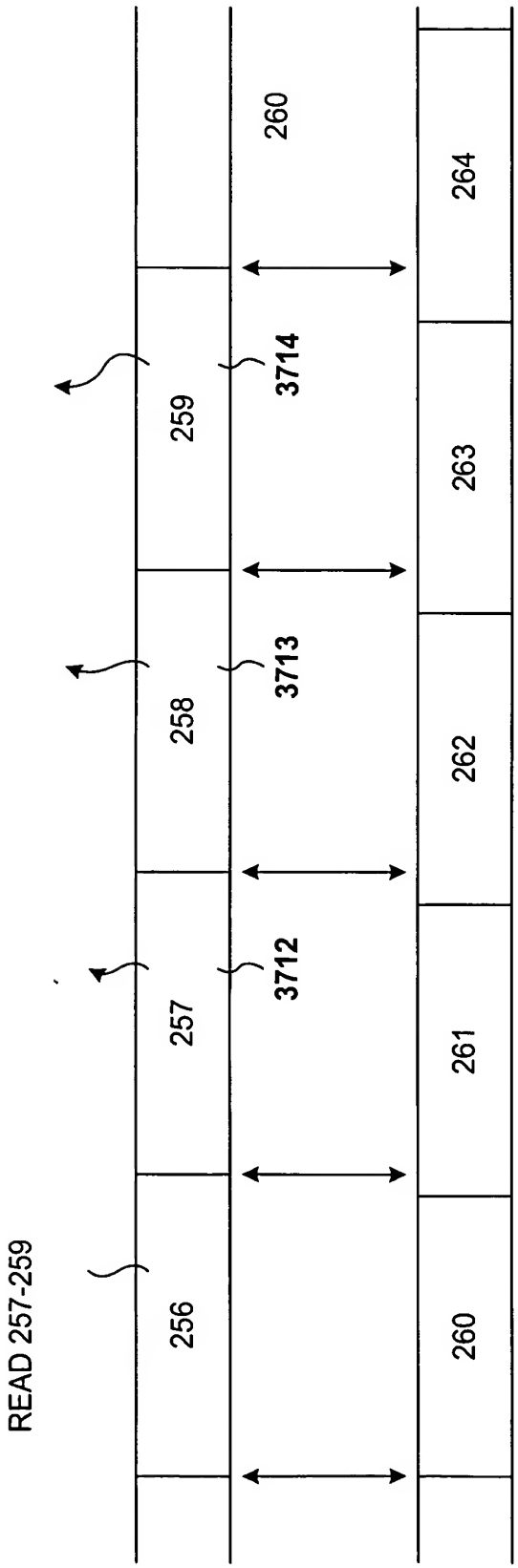


Figure 38A

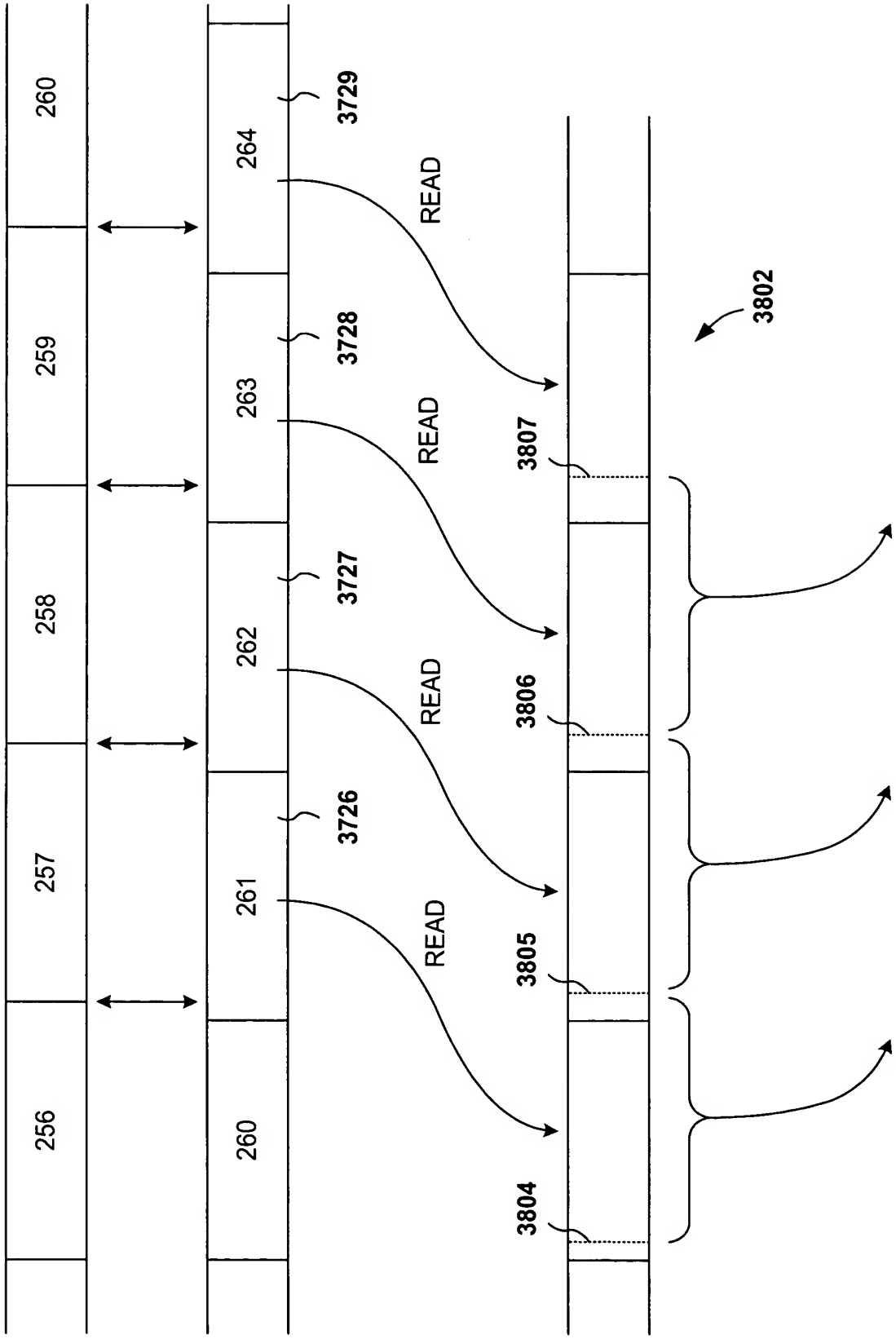

256
257
258
259
260
260
261
262
263
264
3726
3727
3728
3729
READ
READ
READ
READ
3804
3805
3806
3807
3802

Figure 38B

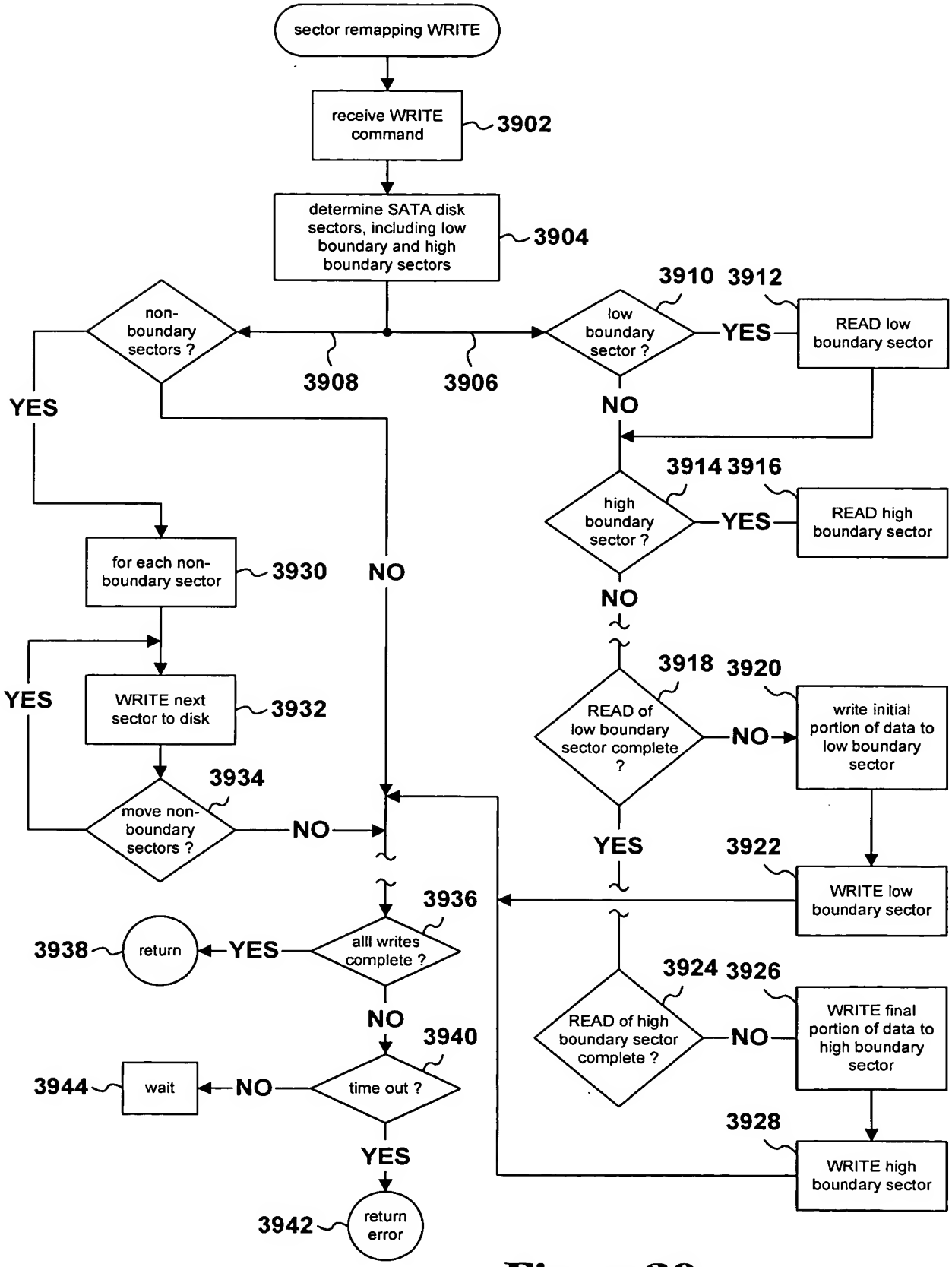

sector remapping WRITE
receive WRITE command
3902
determine SATA disk sectors, including low boundary and high boundary sectors
3904
non-boundary sectors ?
3908
3906
low boundary sector ?
3910
3912
YES
READ low boundary sector
NO
high boundary sector ?
3914
3916
YES
READ high boundary sector
NO
YES
for each non-boundary sector
3930
NO
YES
WRITE next sector to disk
3932
move non-boundary sectors ?
3934
NO
READ of low boundary sector complete ?
3918
3920
NO
write initial portion of data to low boundary sector
YES
3922
WRITE low boundary sector
alll writes complete ?
3936
3938
return
YES
NO
READ of high boundary sector complete ?
3924
3926
NO
WRITE final portion of data to high boundary sector
3928
WRITE high boundary sector
time out ?
3940
3944
wait
NO
YES
3942
return error

Figure 39

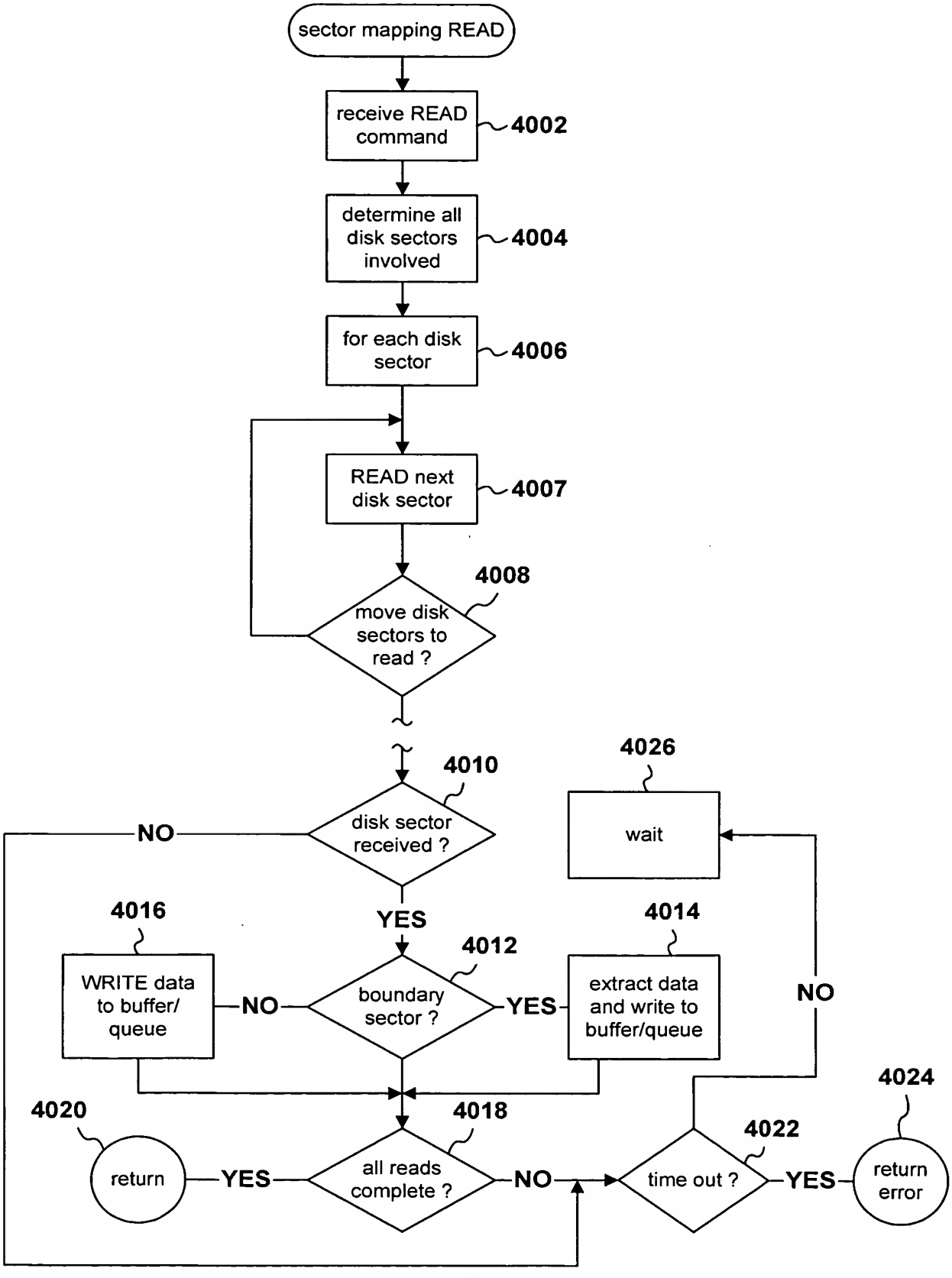

sector mapping READ
receive READ command
4002
determine all disk sectors involved
4004
for each disk sector
4006
READ next disk sector
4007
4008
move disk sectors to read ?
4010
disk sector received ?
NO
YES
4026
wait
4016
WRITE data to buffer/ queue
NO
4012
boundary sector ?
YES
4014
extract data and write to buffer/queue
NO
4024
4020
return
YES
4018
all reads complete ?
NO
4022
time out ?
YES
return error

Figure 40

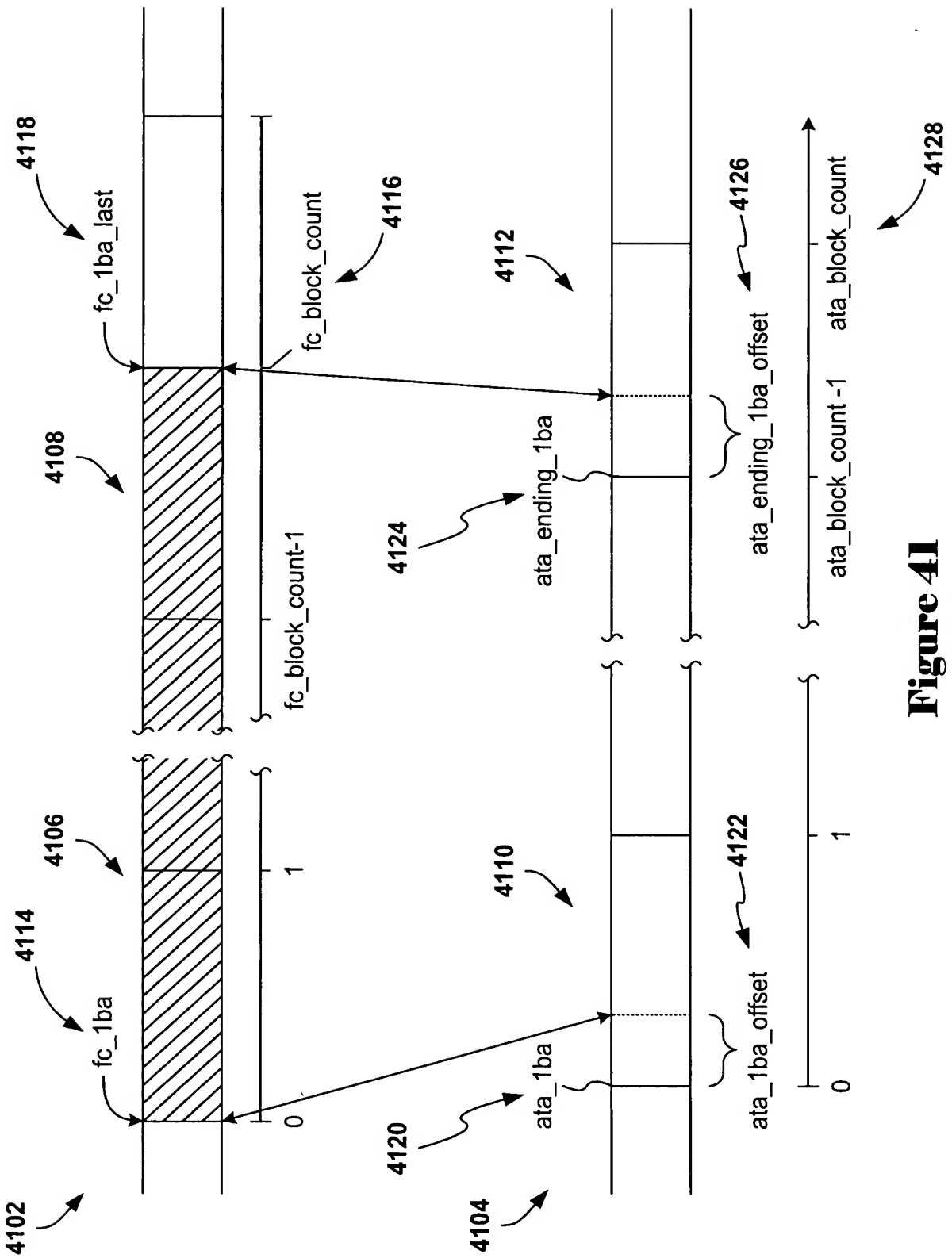

4102
4104
4106
4108
4110
4112
4114
4116
4118
4120
4122
4124
4126
4128
fc_1ba
fc_1ba_last
fc_block_count
fc_block_count-1
ata_1ba
ata_ending_1ba
ata_1ba_offset
ata_ending_1ba_offset
ata_block_count
ata_block_count-1
0
1

Figure 41

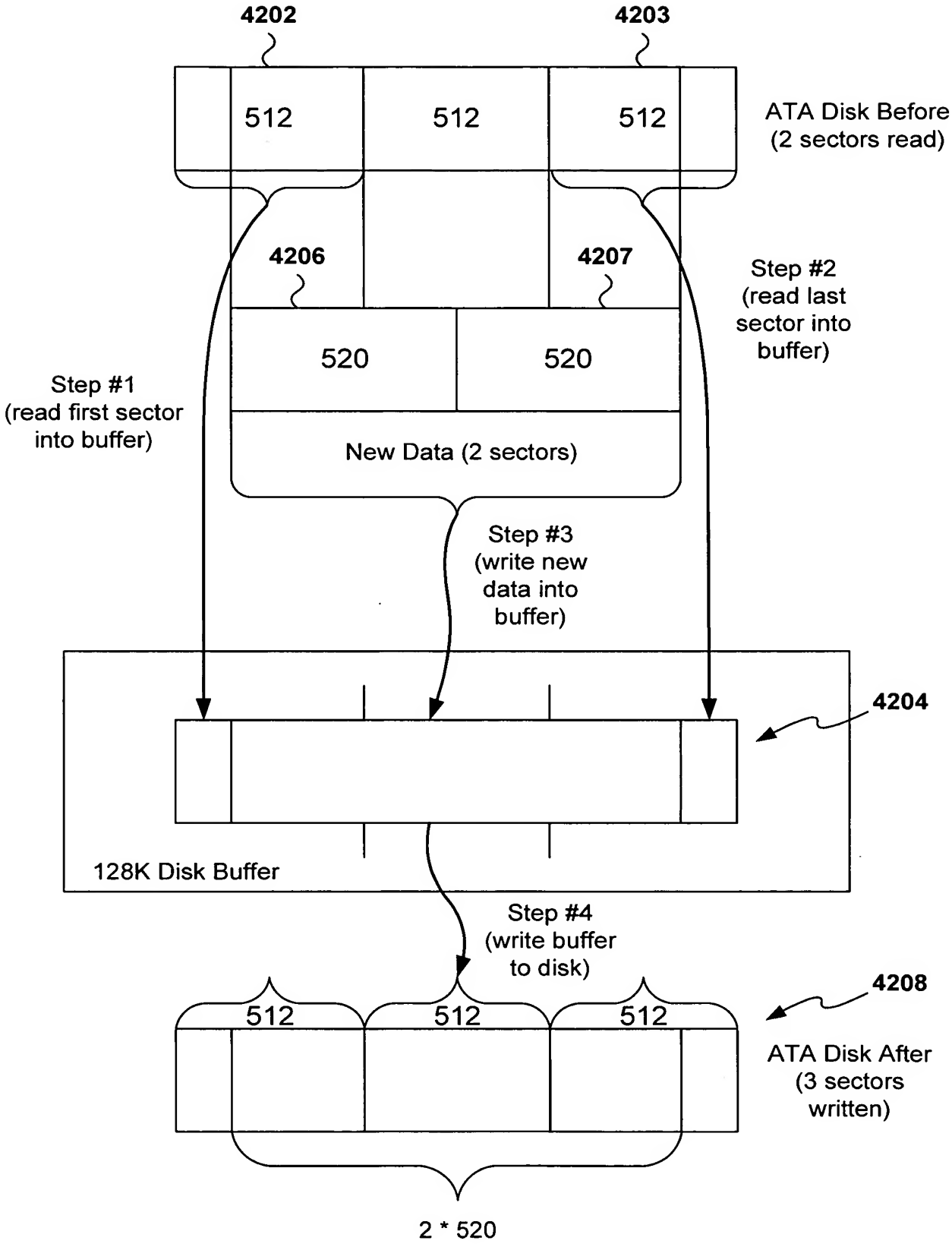

4202
4203
512
512
512
ATA Disk Before
(2 sectors read)
4206
4207
Step #2
(read last
sector into
buffer)
520
520
Step #1
(read first sector
into buffer)
New Data (2 sectors)
Step #3
(write new
data into
buffer)
4204
128K Disk Buffer
Step #4
(write buffer
to disk)
4208
512
512
512
ATA Disk After
(3 sectors
written)
2 * 520

Figure 42

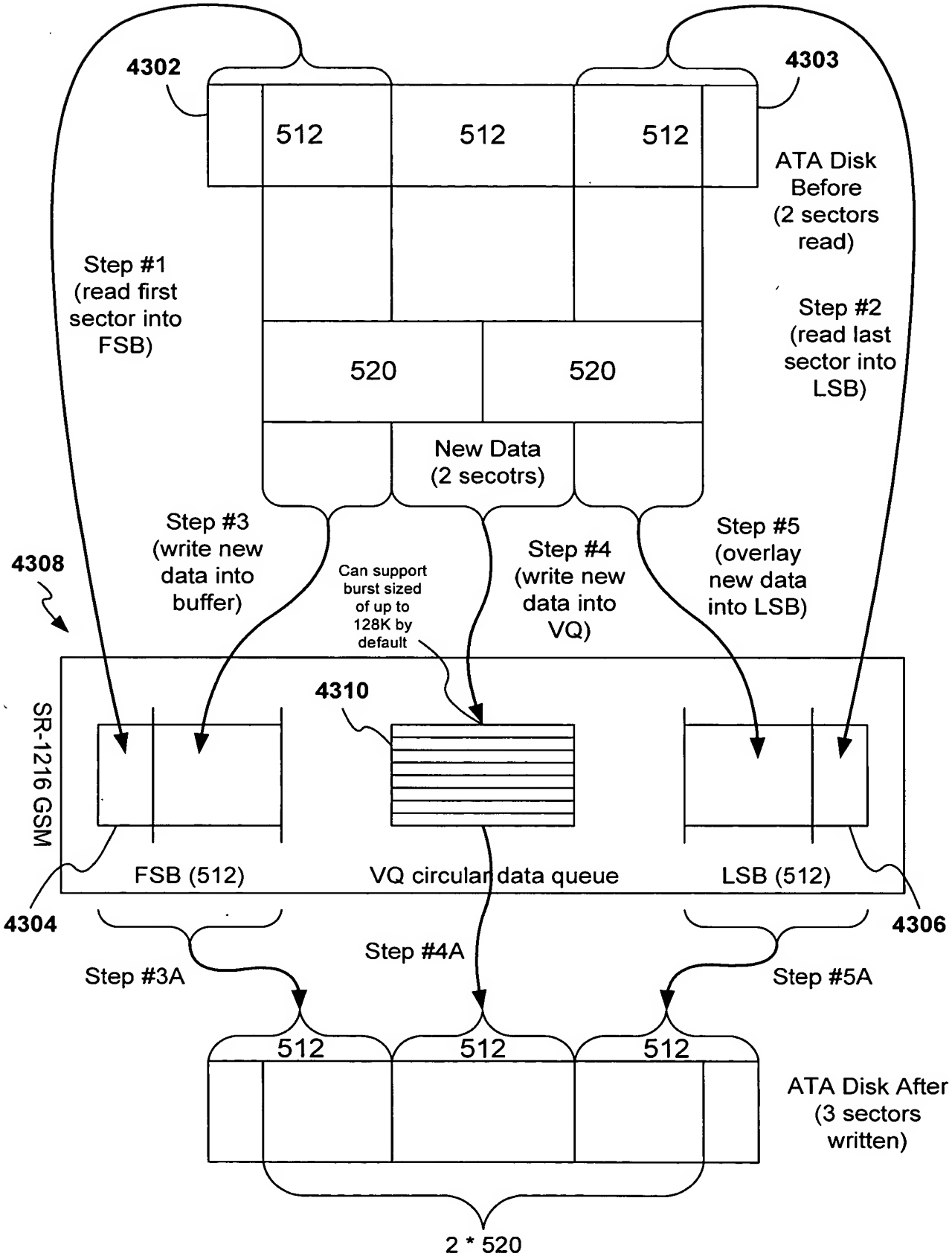

4302
4303
512
512
512
ATA Disk Before (2 sectors read)
Step #1 (read first sector into FSB)
Step #2 (read last sector into LSB)
520
520
New Data (2 secotrs)
Step #3 (write new data into buffer)
Step #4 (write new data into VQ)
Step #5 (overlay new data into LSB)
4308
Can support burst sized of up to 128K by default
4310
SR-1216 GSM
FSB (512)
VQ circular data queue
LSB (512)
4304
4306
Step #3A
Step #4A
Step #5A
512
512
512
ATA Disk After (3 sectors written)
2 * 520

Figure 43

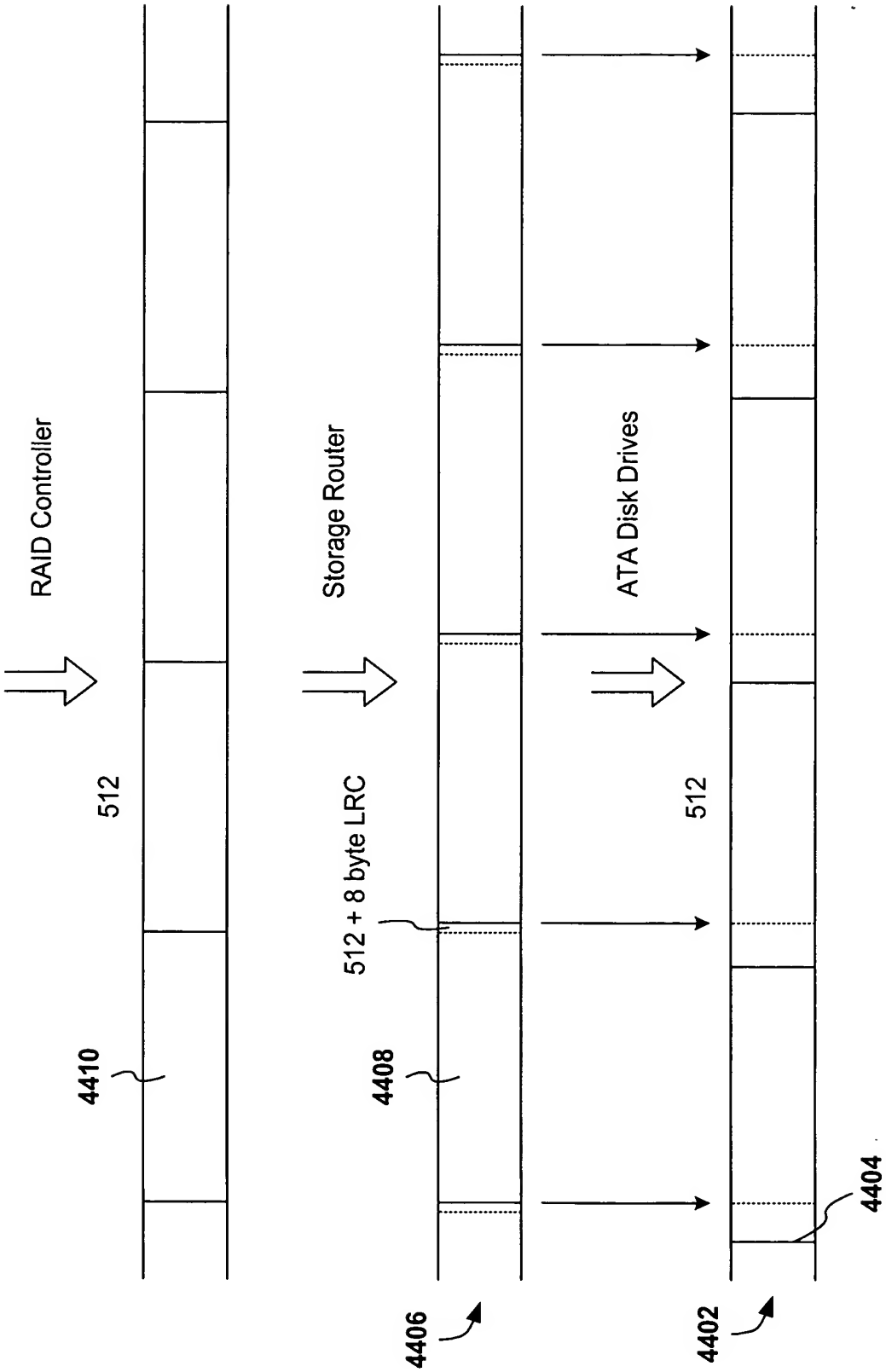

RAID Controller
512
4410
Storage Router
512 + 8 byte LRC
4408
4406
ATA Disk Drives
512
4404
4402

Figure 44

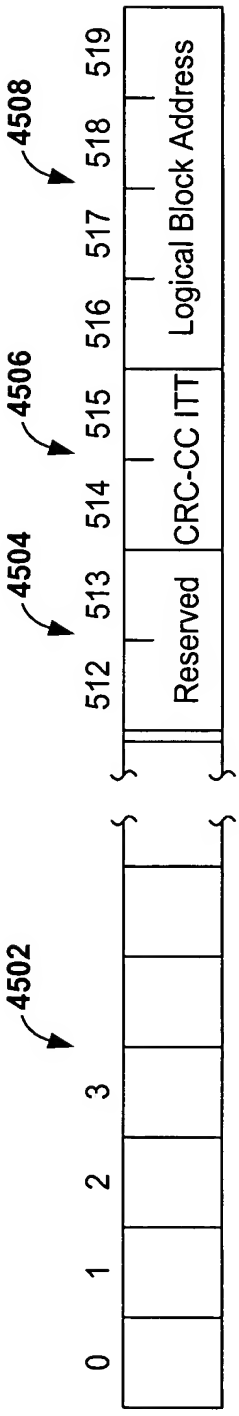
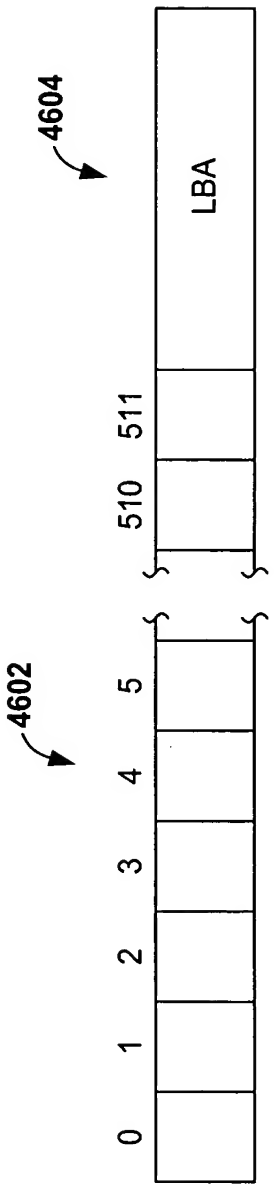


Figure 45



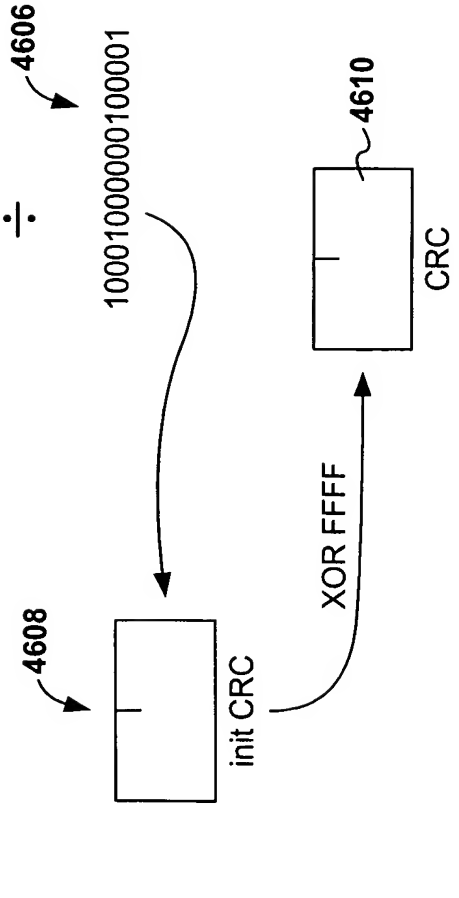


Figure 46

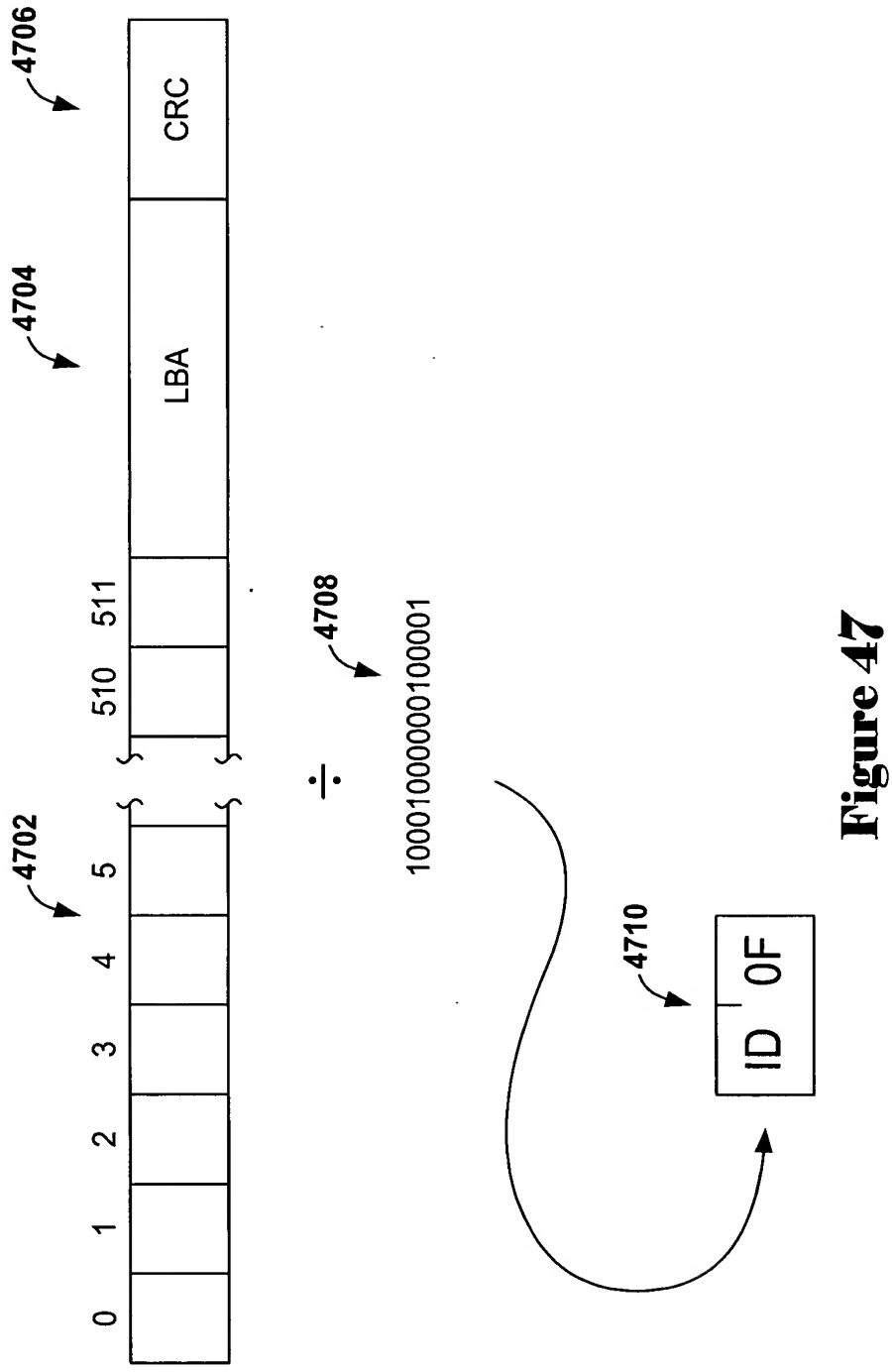

4706
CRC
4704
LBA
511
510
4708
÷
1000100000100001
4702
5
4
3
2
1
0
4710
ID 0F

Figure 47

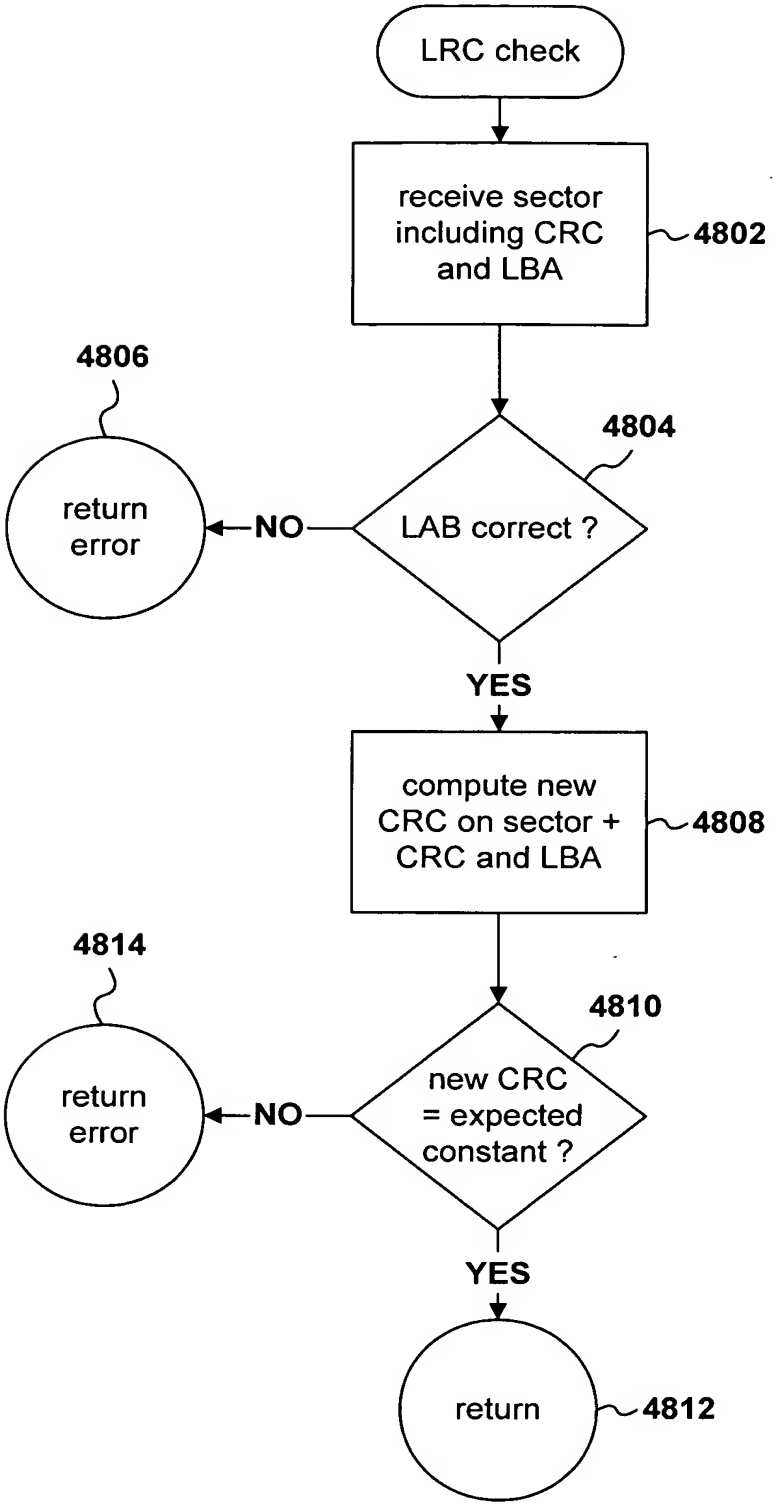

LRC check
receive sector including CRC and LBA
4802
4804
LAB correct ?
NO
return error
4806
YES
compute new CRC on sector + CRC and LBA
4808
4810
new CRC = expected constant ?
NO
return error
4814
YES
return
4812

Figure 48

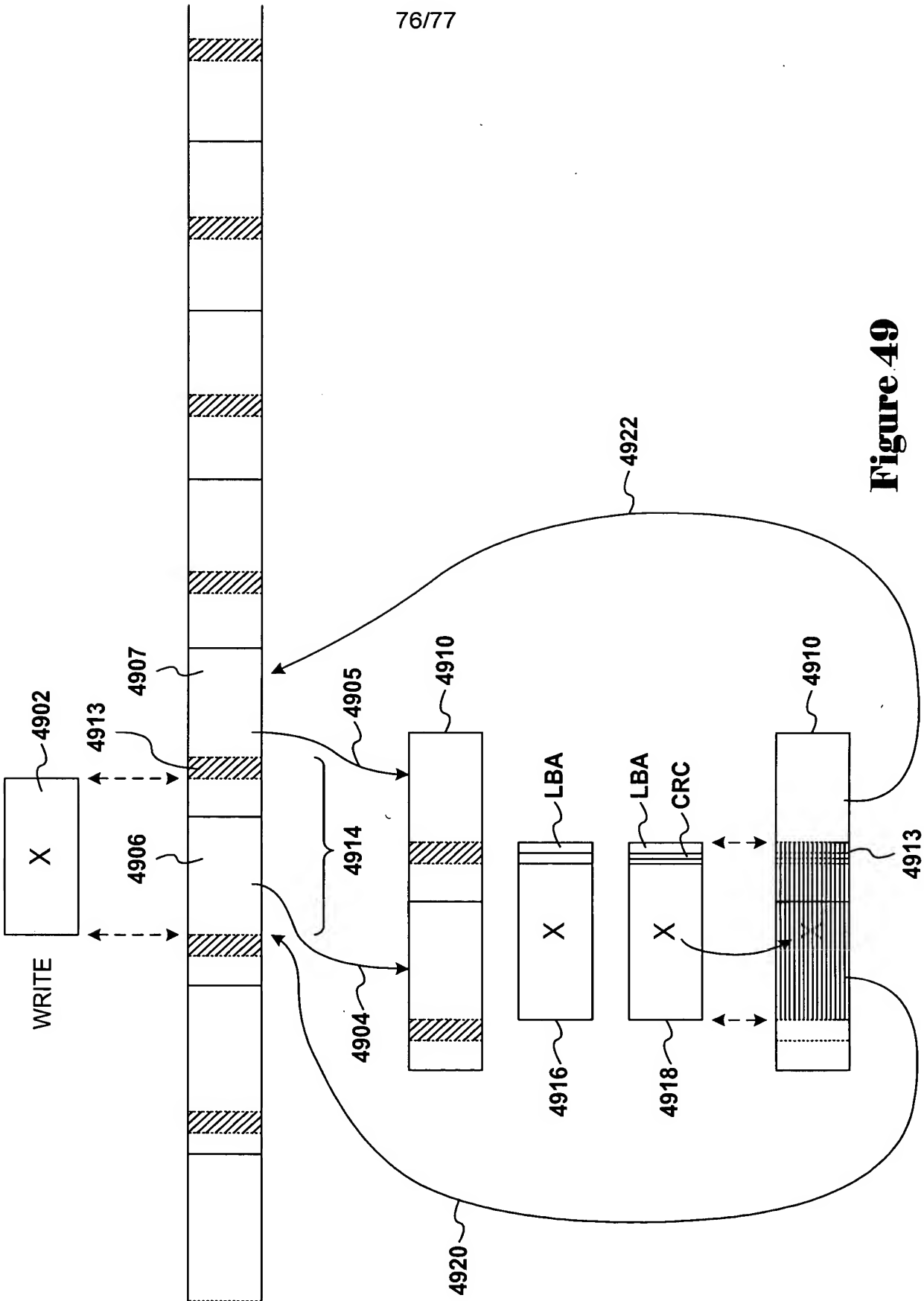

WRITE
X
4902
4913
4907
4906
4914
4905
4904
4910
LBA
X
4916
LBA
CRC
X
4918
4910
4913
4922
4920

Figure 49

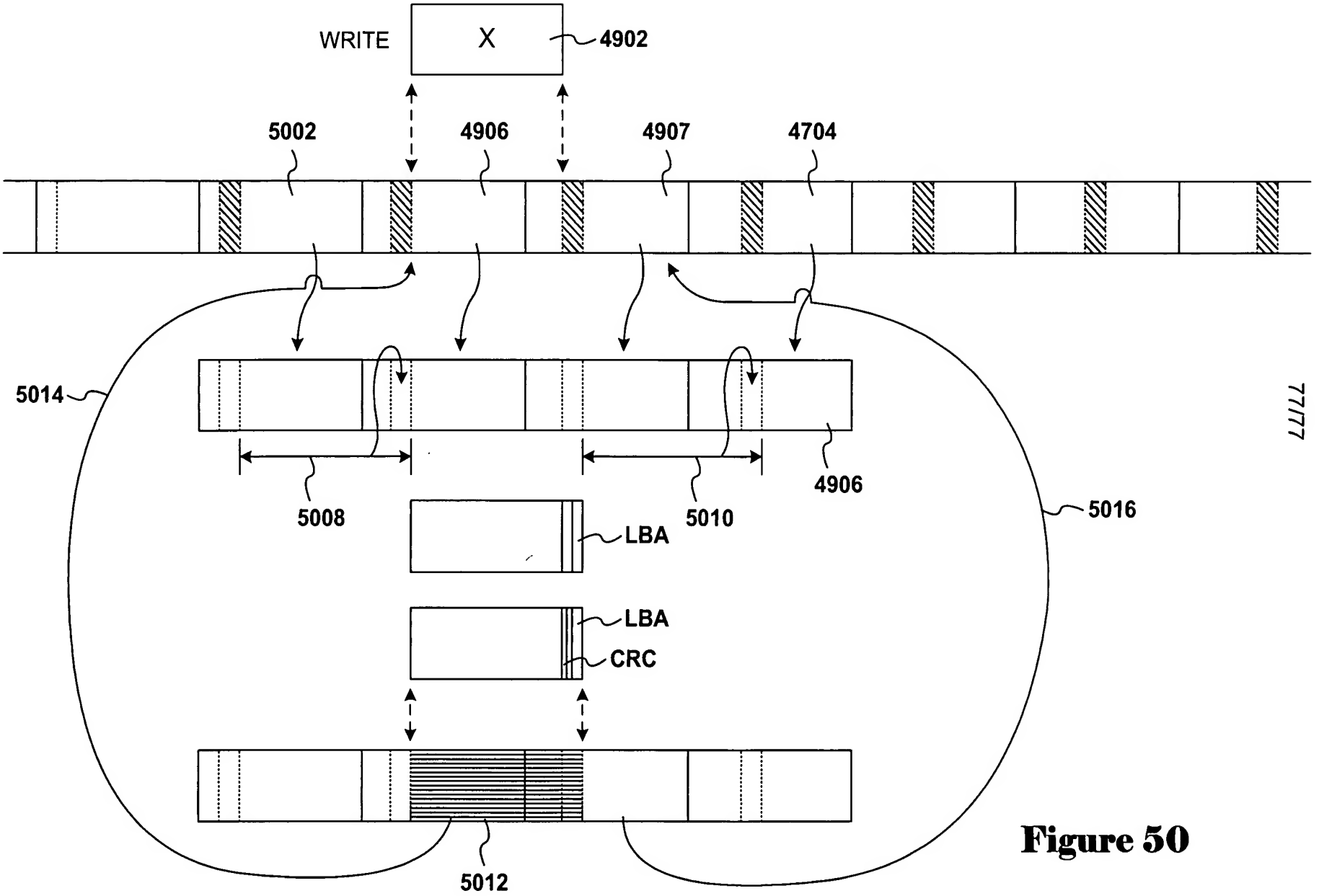

WRITE
X
4902
5002
4906
4907
4704
5014
5008
5010
4906
5016
LBA
LBA
CRC
5012
77177

Figure 50